Description

The SC2422A biphase, current mode controller is designed to work with Semtech smart synchronous drivers, such as the SC1205, SC1305 or the SC1405 to provide the DC/DC converter solution for the most demanding Micro-processor applications. Input current rather than output current sensing is used to guarantee precision phase to phase current matching using a single sense resistor on the input power line. Accurate current sharing and pulse by pulse current limit are implemented without the power loss and transient response degradation associated with output current sense methods. Two phase operation allows significant reduction in input/output ripple while enhancing transient response.

The DAC step size and range are programmable with external components thus allowing compliance with new and emerging VID ranges.

A novel approach implements active droop, minimizing output capacitor requirements during load transients. This avoids the pitfalls of the passive droop implementation. This feature also allows easy implementation of N+1 redundancy and current sharing among modules.

Programmable Under Voltage Lockout assures proper start-up and shutdown by synchronizing the controller to the driver supply. Wide PWM frequency range allows use of low profile, surface mount components.

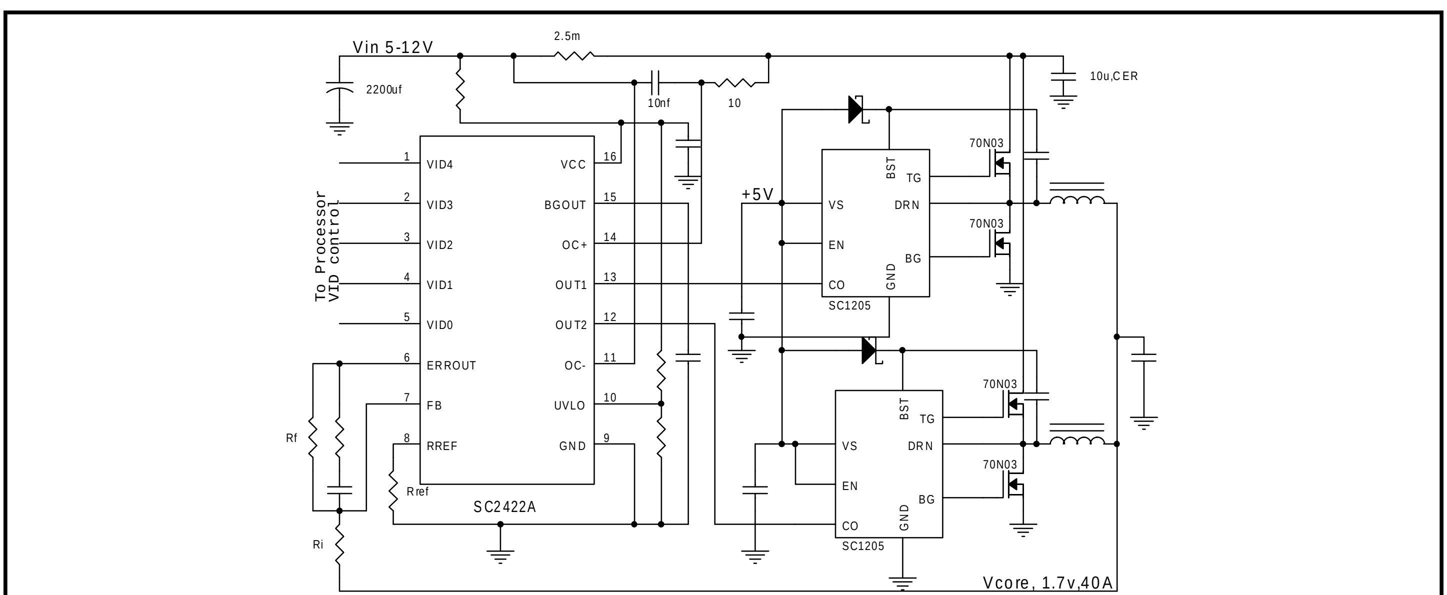
Features

- Precision, pulse by pulse phase current matching
- Active drooping allows for best transient response
- Input Sensing Current mode control
- Programmable DAC step size/offset allows Compliance with VRM9.0, VRM8.3 or VRM8.4
- Externally programmable soft-start
- 5V or 12V input for next generation processors
- 0% minimum duty cycle improves transient response
- Externally Programmable UVLO with hysteresis
- Cycle by cycle current limiting
- Programmable Internal Oscillator to 1 MHz
- VID IIIII Inhibit (No CPU)

Applications

- Intel Advanced Microprocessors
- AMD Athlon™ power supplies
- Servers/Workstations, high density power supplies

Typical Application Circuit



Absolute Maximum Rating

Parameter	Symbol	Maximum	Units
Input DC Rail Voltage to GND	V_{IN}	15	V
PGND to GND		+1	V
Operating Temperature Range	T_A	-20 to 125	°C
Junction Temperature	T_J	0 to 125	°C
Thermal Resistance Junction to Case	θ_{JC}	20	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	60	°C/W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless specified: VCC = +5V, TAMB = 25°C, RREF = 11.5kΩ. See Typical Application Circuit

Parameter	Conditions	MIN	TYP	MAX	UNITS
Chip_Supply					
IC Supply Voltage		4.5	5	14	V
IC Supply Current	V_{CC} = 5.0 ~ 12.0V		9		mA
Reference Section					
Bandgap Output	C_{BG} = 4.7nF		1.5		V
Source Impedance			3		kΩ
Supply Rejection	V_{CC} = 5.0V ~ 12.0V		2		mV/V
VID Step	RI = 6.49kΩ, RREF = 11.5kΩ		25		mV
Voltage Accuracy		-1		1	%
Temperature Stability	0°C < T_{AMB} < 70°C		5		%
Voltage Accuracy	0°C < T_{AMB} < 70°C		+/-1		%
Oscillator Section					
Frequency Range		400		1000	kHz
Frequency Accuracy	V_{IN} = 12.0V, R_{REF} = 13kΩ or V_{IN} = 5.0V, R_{RE}F =11.5kΩ	450	500	550	kHz
Temperature Stability	0°C < T_{AMB} < 70°C		+/-5		%
Voltage Error Amplifier					
Input Offset Voltage			+/-5		mV
Input Offset Current			0.1		µA
Open Loop Gain	1V < V_{ERROUT} < 4V		90		dB
PSRR	V_{CC} = 5 - 12V		80		dB
Output Sink Current	V_{ERROUT} = 1V		2.5		mA
Output Sink Current	V_{ERROUT} = 1V		2.5		mA
Unity Gain Bandwidth	I_O < 100µA		5		MHz
Slew Rate	I_O < 100µA		10		V/uS
Current Sense Amplifier					
Amplifier Gain	(V_{OC-} - V_{OC+}) < 100mV		26		dB

Electrical Characteristics

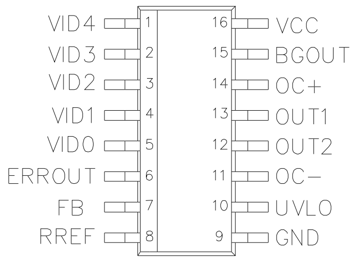
Unless specified: VCC = +5V, TAMB = 25°C, RREF = 11.5kΩ. See Typical Application Circuit

Parameter	Conditions	MIN	TYP	MAX	UNITS
Input Offset Voltage, Input Referred	$(V_{OC-} - V_{OC+}) < 100mV$		4		mV
CMRR	V_{ICM} = 9 ~ 14V @ DC		80		dB
PSRR	V_{CC} = 9 ~ 14V @ DC		80		dB
Input Common Mode Range			VCC +/- 0.3		
Max Differential Signal/ Current Limit Threshold	$V_{OC-} - V_{OC+}$		100		mV
Protection					
UVLO Threshold	R_{SOURCE} UVLO pin = 20kΩ		1.33		V
UVLO Hysteresis Current	R_{THEV} = 10kΩ		6		µA
Outputs (OUT 1, OUT 2)					
Max Duty Cycle	Per phase, F_{OSC} = 500kHz		47		%
Duty Match	F_{OSC} = 500kHz	-.5		.5	%
Typical Output Voltage Swing	R_L = 10kΩ	.8		2.5	V
	R_L = 100kΩ	.2		3.3	V
VID Logic Threshold		0.8		2	V
VID Logic Pin Bias Current	V_{IN} = 0		12		µA

Note: (1) If the VID pins are driven high by an external source (in contrast to being left open), then all VIDs input will need to be externally pulled high. If VIDs are left open, no external pull-up is required.

Pin Configuration

Top View



(16-Pin SOIC)

Ordering Information

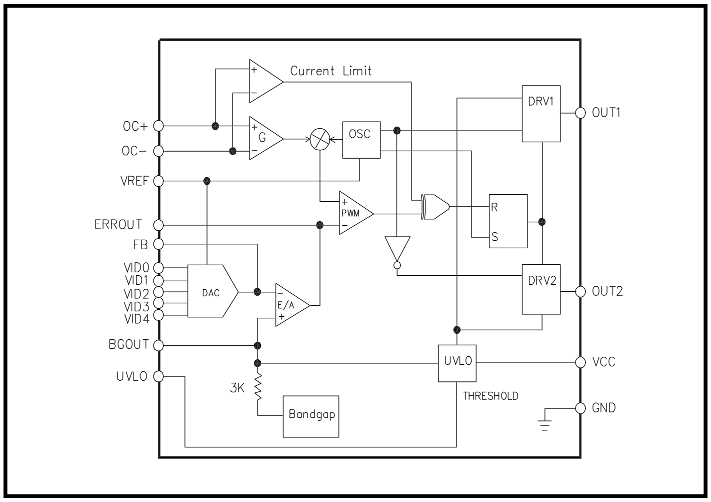
Device[(1)]	Package	Temp. Range(T_J)
SC2422ACS.TR	SO-16	0 - 125°C
SC2422A.EVB	Evaluation Board	

Note: (1) Only available in tape and reel packaging. A reel contains 1000 devices.

Pin Descriptions

Pin 1: VID4 , MSB
Pin 2: VID3
Pin 3: VID2
Pin 4: VID 1
Pin 5: VID0 , LSB
Pin 6: ERROUT Error-amplifier output.
Pin 7: FB Error-amplifier inverting input.
Pin 8: RREF Frequency setting resistor pin. Also programs the DAC current step size. (see application information for programming the frequency)
Pin 9: GND Chip ground.
Pin 10: UVLO Programmable Under Voltage Lock-Out. This pin may be connected to the MOSFET driver supply through a voltage divider to inhibit the SC2422A until the drivers are on. The UVLO comparator trip point is 1.33V (typical).
Pin 11: OC- Input current sense, negative input. This pin is connected to the input supply side of the current sense resistor.
Pin 12: OUT2 PWM output for phase 2. Drives external Power MOSFET driver.
Pin 13: OUT1 PWM output for phase 1. Drives external Power MOSFET driver.
Pin 14: OC+ Input current sense positive input. This pin is connected to MOSFET side of the current sense resistor.
Pin 15: BGOUT Soft start and reference. Bypass to ground with a .022µF - 0.1µF capacitor to implement soft start in conjunction with internal 3KΩ resistor. To ensure output voltage accuracy, the maximum current source/sink from this pin should be limited to 0.5 uA.
Pin 16: VCC Chip positive supply.

Block Diagram



Applications Information

OUTPUT VOLTAGE (VRM 9.0) Unless specified: 0 = GND; 1 = High (or Floating) T_A = 25°C, V_{CC} = 5V, 2-Phase operation					V_{CCCORE}
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**(VDC)**
1	1	1	1	1	Output Off
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

Applications Information (Cont.)

The SC2422A is an Input Current Mode Controller designed for High Current, High performance two phase DC/DC converters. The Current mode control is implemented by generating the PWM ramp from the Input Current, rather than the output current. This has the advantage of eliminating the output current sense resistors, and the power loss associated with output current sensing. Eliminating the output current sense resistors has the added advantage of improving the transient response by reducing the output impedance.

The output voltage is programmed via a 5-bit DAC in 32 steps. A novel technique allows programmable DAC step size and output offset, allowing the SC2422A based DC/DC converters to work in VRM9.0, VRM 8.3, VRM8.4, VRM8.5 or future specified voltage ranges.

Theory of Operation
Pulse by Pulse Current Matching

The operation of the Input Current Mode, ICM, is as follows:

The SC2422A Oscillator generates the OUT1 and OUT2 logic output drives. OUT1 and OUT2 are non-overlapping and sequentially command an external, power MOSFET driver to turn on the Top MOSFETs. When the Top MOSFET is enhanced (each phase), the input voltage is impressed across the MOSFET and the output Inductor. The AC current in the inductor is:

$$IL = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L} = \frac{(V_{IN} - V_{OUT}) \times D}{FxL}$$

Where F is the frequency (per phase) and L is the output inductor. D is the duty cycle and is approximately equal to V_O/V_{IN}. The approximation arises from the fact that the Duty cycle extends slightly to compensate for losses in the current path. These losses include RDS_ON of the MOSFET, the Equivalent Series Resistance of the Inductors and the PCB trace resistances.

The inductor current flows in the input current senseresistor, generating a PWM ramp, same as in all current mode controllers. The ramp is compared with an amplified, level shifted and filtered version of the output voltage at the PWM comparator. The comparator then outputs a gate drive pulse that terminates when the ramp voltage equals the error amplifier output signal.

The current mode control is inherently immune to input

voltage changes because the ramp amplitude reflects the input voltage changes.

Since the input current sense resistor is the same for both phases, the inherent inaccuracy due to mismatch between output current sense resistors is avoided. Also, since the comparator threshold is the same for both phases, accurate current matching is achieved between phases. This implements a pulse by pulse current matching with a faster response to changes in output current by monitoring the input current for each phase.

Programming the SC2422A

Figure 2 below, is the connection schematic for the Internal Error Amplifier.

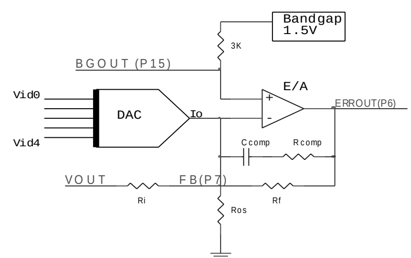


Figure 2: Error amplifier connections

The external components, R_I, R_{OS} and R_F set the DAC step size, output voltage offset and droop, accordingly. A resistor from R_{REF} (pin 8) to ground programs the frequency as well as the DAC *current* step size.

Programming the Switching Frequency

The oscillator frequency can be selected first by setting the value of R_{REF} resistor (pin 8) to ground.

$$f_{OSC} = \frac{13k\Omega * 500kHz}{R_{REF}}$$

$$V_{IN} = 12V$$

The switching frequency per phase is 1/2 of the oscillator frequency.

Programming the DAC Step Size

The SC2422A allows programming the output voltage and the DAC step size by selecting external resistors.
The DAC *current* step size, for one MSB is:

$$I_{DAC\_MSB} = \frac{V_{BG}}{R_{REF}}$$

where R_{REF} is the resistor from R_{REF} pin to Ground.

The DAC MSB *voltage* step size is calculated as follows:
$V_{DAC\_MSB} = I_{DAC\_MSB} * R_I$

$$V_{DAC\_LSB} = \frac{V_{DAC\_MSB}}{32}$$

or

$$V_{DAC\_LSB} = \frac{V_{BG} * R_I}{V_O * V_{BG}} \times \frac{R_I}{32}$$

Note that changing R_{REF} affects both frequency and DAC step size. R_I must be proportionally adjusted to keep the same step size at different frequencies. The advantage of this method is that all new VID specifications can be accommodated by modifying external components while maintaining the required precision without the need for converter redesign.

Programming the DAC Offset Voltage

Kirchoff's current law can be applied to the error amplifier's Inverting node (see figure 2) to calculate R_{OS}, the DAC offset setting resistor. The output Offset at zero DAC current (VID=00000), is set as follows:

$$R_{OS} = \frac{V_{BG} * R_I}{V_O - V_{BG}}$$

Where V_{BG} = Precision Reference Voltage = 1.50V. The value of R_{OS} can be fine trimmed using a potentiometer connected from the FB pin to ground.

Programming the Dynamic (Active) Droop

The SC2422A employs a novel approach to active drooping for optimum transient response. The output voltage is regulated as a function of output current. At zero current the output is regulated to the upper limit of the output voltage specification. As the load is increased, the output "droops" towards the lower limit. This makes optimum use of the output voltage error band, yielding minimum output capacitor size and cost.
Active drooping, does not compromise the converter response time as does passive droop techniques. The active droop also allows for an accurate Inter-Module current sharing scheme, where multiple DC/DC converters are required to share the current required by a DC bus. As one module supplies more current, that modules output voltage "droops", allowing other modules to provide the balance of the required current. Any changes in the output voltage is instantaneously reflected to the error amplifier, which has a high slew rate and wide Gain-Bandwidth product to recover the output voltage to its nominal level with minimal delay.

The droop is adjusted by setting the feedback resistor, Rf. While the optimum value of R_F may be derived experimentally, the following equation can provide the droop at a given output current:

$$V_{DROOP} = \frac{G_{CA} * R_I * R_S * I_{OUT}}{2_{RF}}$$

The Gain of the current amplifier, G_{CA}, is set to 20 (26dB), while R_S is the input sense resistor.

The effective inductance of the sense resistor and the sensing path must be minimized to achieve accurate correlation between the above equation and actual droop achieved. The value of R_F may have to be adjusted to compensate for such parasitic effects.

Since Rf also sets the DC gain of the system, changing the value of Rf affects the offset voltage, which is set via Ros. The value of Ros can be modified to achieve exact offset after the droop resistor has been chosen.

It must be noted that the Current Amplifier gain is quite precise, with greater than 80dB of Common Mode Rejection Ratio (CMRR). Thus the droop's accuracy is limited primarily by external components tolerances and the external parasitic effects.

Applications Information(Cont.)

Loop Gain Considerations

The Modulator gain in Input Current Mode control is equal to:

$$K_{MOD} = \frac{V_{IN}}{V_{RAMP}}$$

$$V_{RAMP} = 0.3V + R_{SENSE}\ X\ T_{OSC}\ X\ G_{CA}\ X\ \frac{V_{IN} - V_O}{L}$$

Where:
R_S = Input current sense resistor
T_{OSC} = Oscillator period
G_{CA} = Current Amplifier Gain
0.3V is the ramp added for slope compensation when the output current is near zero.

The DC loop gain is the product of the modulator gain and the error amplifier gain and is calculated as follows:

$$G_{LOOP} = \frac{V_{IN} * R_F}{V_{RAMP} * R_I}$$

Programming the Under Voltage Lockout

The Under Voltage Lockout (UVLO) may be programmed using an external voltage divider. An internal current programs the hysteresis. The hysteresis current vanishes once the controller has turned on. Thus the ramp-down threshold can be calculated first from Figure 2 as follows:

Vcc (ramp-down) = Vn • (1+R1/R2)

Vn is the voltage at the inverting input and equals the voltage at the non-inverting input just before tripping. (When this voltage is reached the converter will shut down). The comparator Ramp up Voltage, (as Vcc is increased) just before tripping, must take into account the hysterisis.

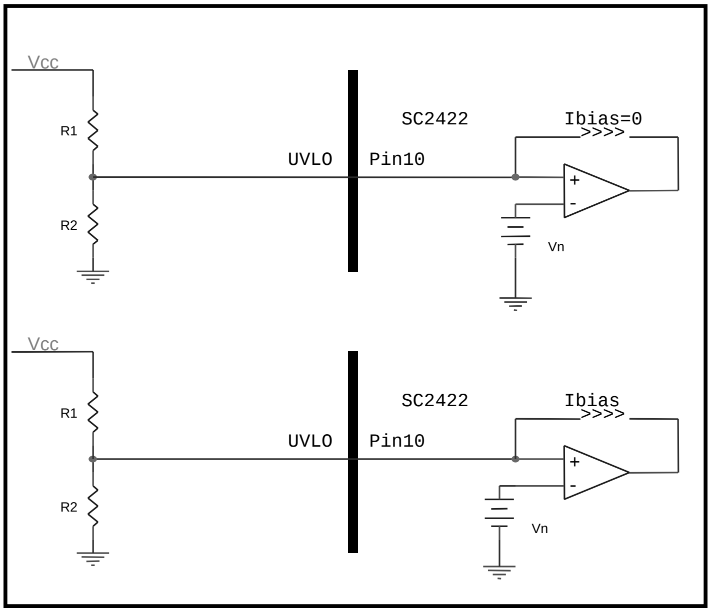
The Norton equivalent for Figure 3 yields the following equation for the Ramp up trip point:

Vcc (ramp-up) = Vn • (1+R1/R2) + I_{BIAS} • R1

where: Vn = 1.33V and I_{BIAS} = 6µA.

The resistor, Vn and Ibias tolerances will affect the actual trip point and should not be ignored if tight UVLO control is desired. In reality, the worst case errors accumulate in an RMS fashion (and not additive) and the Vcc UVLO behavior can be predicted accordingly.

The UVLO setting should consider external MOSFET driver's UVLO threshold. Ideally, the external MOSFET driver should turn on before the SC2422 controller and turn off before the controller. This assures the converter output will rise and fall slowly using the soft start feature of the SC2422 and that the output voltage will not go negative at turn-off.



SC2422A Evaluation Board

The SC2422A based DC/DC converter utilizes the SC1205 High Speed MOSFET drivers to achieve VRM 9.0 output Voltage Specifications. SC2422A Evaluation Board Schematic (Figure 1) shows the circuit for a 40A, BiPhase DC/DC converter. The Evaluation board is available by contacting the factory or Semtech website at WWW.Semtech.com.

Typical Characteristics

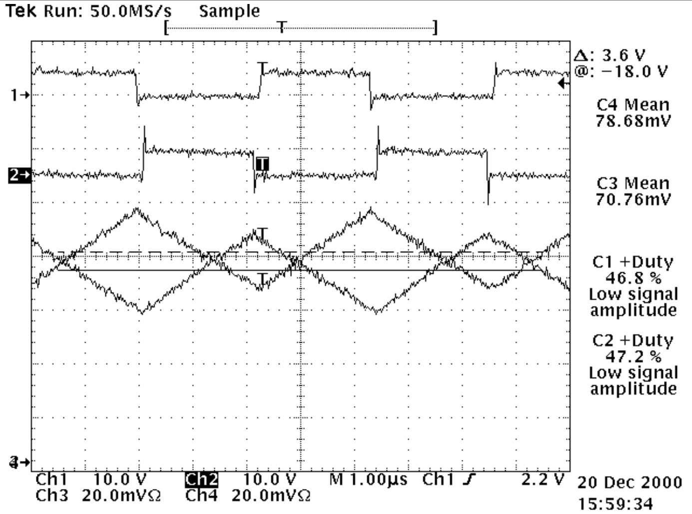


Figure 1: Output current of 30A is shared between the two phases. (delta I<1A for a 30A output @1.7V).
Ch1: Phase node of phase 1
Ch2: Phase node of phase 2
Ch3: Inductor current , phase 1
Ch4: Inductor current , phase 2

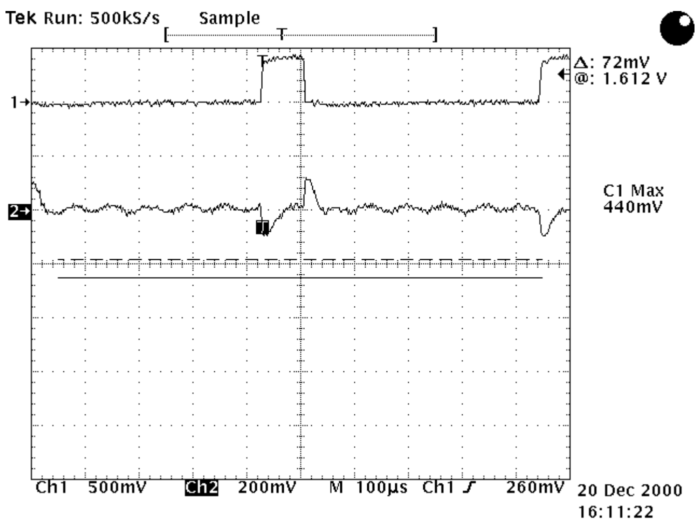


Figure 2: Response of the supply to 44A transient with components as per schematic in figure 5. Iout DC=3A,
Ch1: Transient current sensed across a 10 milliohm resistor (50A/div)
Ch2: Supply Output voltage (Offset=1.7V)

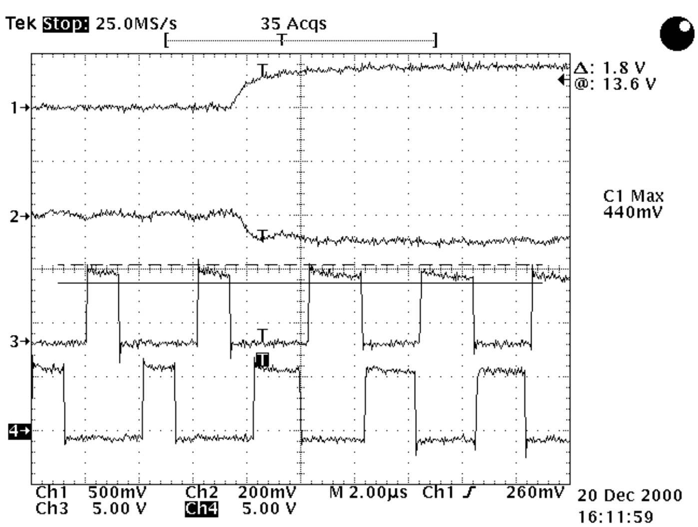


Figure 3: Response of the supply to 44A transient with components as per schematic in figure 5. Iout DC=3A, Time expanded with phase nodes response shown. Note the pulse width increases in less than 1usec, verifying loop recovery speed.
Ch1: Transient current sensed across a 10 milliohm resistor (50A/div), rise time.
Ch2: Supply Output voltage (Offset=1.7V)
Ch3,Ch4: Phase nodes

Typical Characteristics (Cont.)

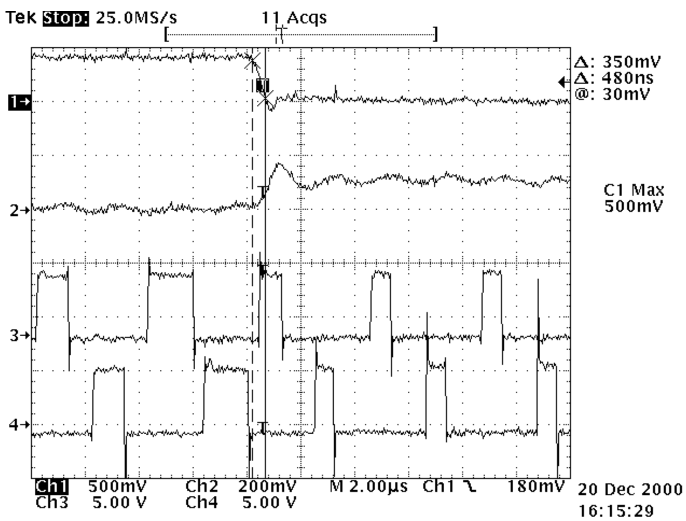
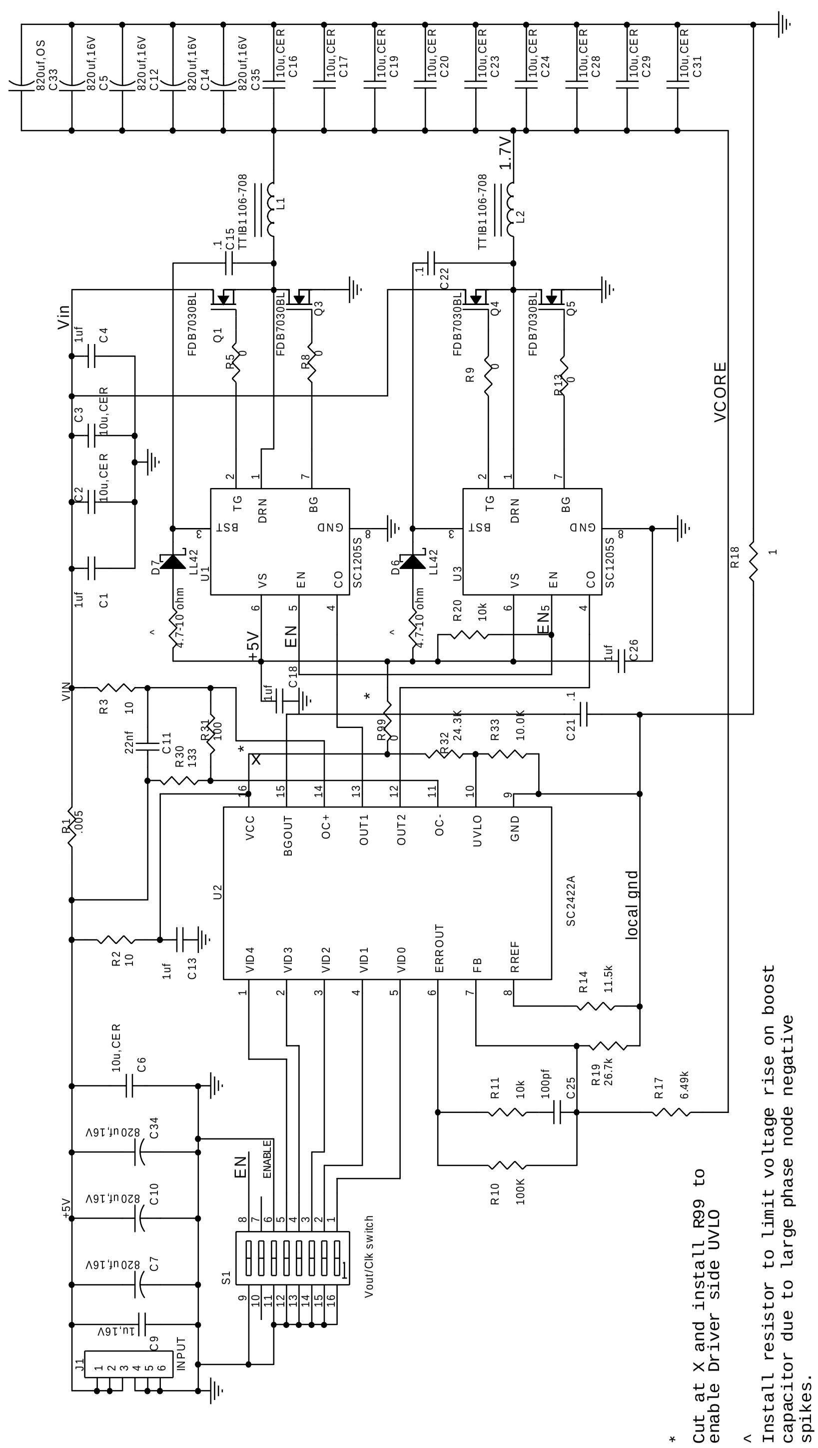


Figure 4: Response of the supply to 44A transient with components as per schematic in figure 5. Iout DC=3A, Time expanded with phase nodes response shown. Ch1 current speed is measured with cursor to equal 35A/480ns=73A/usec. Note the pulse width decreases in less than 1usec.
Ch1: Transient current sensed across a 10 milliohm resistor (50A/div), rise time.
Ch2: Supply Output voltage (Offset=1.7V)
Ch3,Ch4: Phase nodes

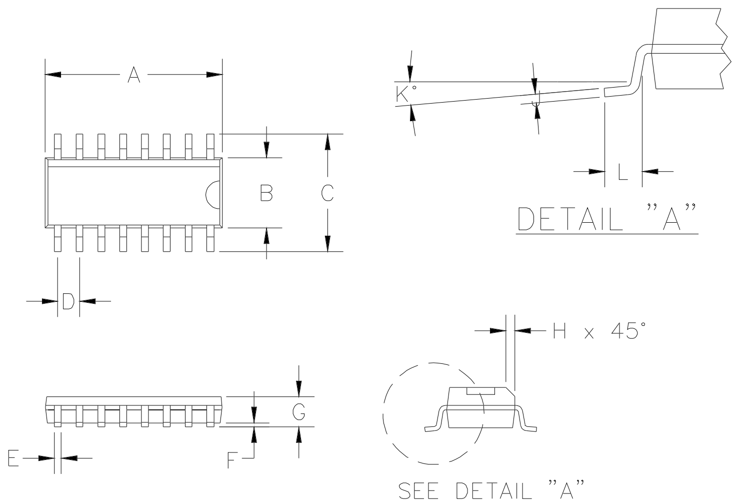
Figure 5- Microprocessor Core Supply Evaluation Board Schematic



Bill of Materials

Item	Qty	Reference	Part Number/Value	Manufacturer
1	5	C1,C4,C13,C18,C26		
2	12	C2,C3,C6,C16,C17,C19,C20, C23,C24,C28,C29,C31	10u,CER	
3	7	C5,C7,C10,C12,C14,C34, C35	820uf,16V	Panasonic
4	1	C9	1u, 16V	
5	1	C11	22nf	
6	3	C15, C21, C22	.1	
7	1	C25	100pf	
8	1	C33	820uf, OS	Sanyo
9	2	D7, D6	LL42	
10	1	J1		
11	2	L2, L1	TTIB1106-708, 700nh	FALCO
12	4	Q1, Q3, Q4, Q5	FDB7030BL	Fairchild
13	1	R1	.005	
14	2	R2, R3	10	
15	5	R5, R8, R9, R13, R99	0	
16	1	R10	100K	
17	2	R11, R20	10k	
18	1	R14	11.5k	
19	1	R17	6.49k	
20	1	R18	1	
21	1	R19	26.7k	
22	1	R30	133	
23	1	R31	100	
24	1	R32	24.3K	
25	1	R33	10.0K	
26	1	S1		
27	2	U3, U1	SC1205	
28	1	U2	SC2422A	
29	1	optional	4.7-10 ohm	

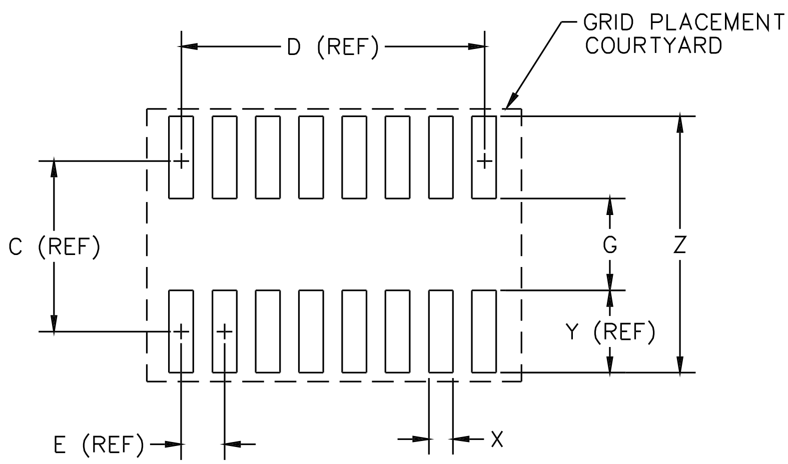
Outline Drawings - SO-16



DIMᴺ	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.386	.393	9.80	10.0	2
B	.150	.158	3.80	4.00	2
C	.228	.244	5.80	6.20	–
D	.050	BSC	1.27	BSC	–
E	.013	.020	0.33	0.51	–
F	.004	.010	.10	.25	–
G	.053	.069	1.35	1.75	–
H	.010	.020	.25	.50	–
J	.007	.010	.19	.25	–
K	0°	8°	0°	8°	–
L	.016	.050	.40	1.27	–

(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS

Land Pattern - SO-16



DIMᴺ	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.197	–	5.00	–
D	–	.35	–	8.89	–
E	–	.05	–	1.27	–
G	.102	.110	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.095	–	2.40	–
Z	.28	.29	7.20	7.40	–

(1) GRID PLACEMENT COURTYARD IS 22 X 16 ELEMENTS (11mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

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