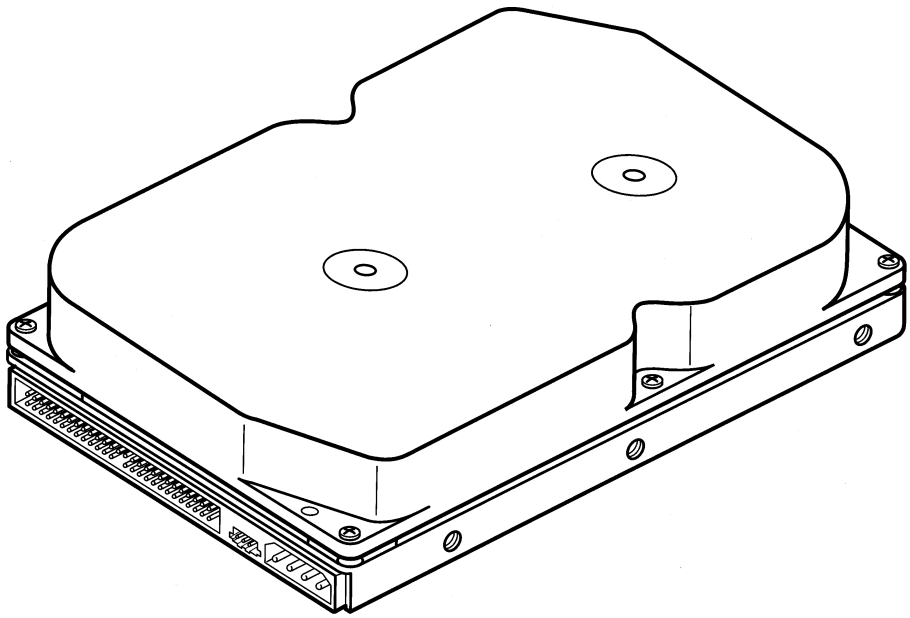
SAMSUNG

Technical Manual

3.5” Hard Disk Drives

Winner 3A / 2A
WA31273A / WA32543A
WA33203A / WA31083A
WA32163A / WA32162A



FEBRUARY,1998(REV.D)

Winner 3A
WA31273A / WA32543A / WA33203A
WA31083A / WA32163A

Winner 2A WA32162A

OEM Technical Manual

This TECHNICAL MANUAL may contain some technical inaccuracies or typographical errors. Changes are periodically made to the information herein, these changes will be incorporated in new editions of this publication. SAMSUNG may make improvements and/or changes in the product(s) described in this publication at any time.

Requests for technical information about this product to SAMSUNG Electronics, Storage System Division, 94-1 IM SOO-DONG, KUMI CITY, KYUNG BUK, KOREA.

Trademark Acknowledgments

Chapter 1
SCOPE

This chapter gives an overview of the contents of this manual, including the intended user, manual organization, terminology and conventions. In addition, it provides a list of other references that might be helpful to the reader.

1-1 *User Definition*

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A technical manual is intended for the following readers:

- Original Equipment Manufacturers (OEMs)
- Distributors

1-2 *Manual Organization*

This manual provides information about installation, principles of operation, and interface command implementation. It is organized into the following chapters:

- Chapter 1 - Scope
- Chapter 2 - Overall Description
- Chapter 3 - Specifications
- Chapter 4 - Installation and Operation
- Chapter 5 - Disk Drive Operation
- Chapter 6 - AT Interface and ATA Commands
- Chapter 7 - Maintenance

In addition, this manual contains a glossary of terms to help you understand important information.

1-3 *Terminology and Conventions*

The abbreviations listed below are used in this manual

µinches	Microinches(10^{-6} inches)
µs	Microseconds
BPI	Bits per inch
dB	Decibels
FCI	Flux changes per inch
GB	Gigabytes
Hz	Hertz
Kbytes	Kilobytes
lbs	Pounds
M	Meter
mA	Milliampere
MB	Megabytes
Mbit/s	Megabits per second
Mbytes/s	Megabytes per second
MHz	Megahertz
mil	Millinches
ms	Milliseconds
mV	Millivolts
ns	Nanoseconds
RPM	Rotations per minute
TPI	Tracks per inch
V	Volts
W	Watts

This manual uses the following convention:

- **Computer Message**

  Computer message refers to items you type at the computer keyboard. These items are listed in all capitals in Courier New font. For example:

  ```
  FORMAT C:/S
  ```

- **Commands and Messages**

  Interface commands and messages sent from the drive to the host are listed in all capitals. For example:

  READ CONFIGURATION
  WRITE LONG

- **Parameters**

  Parameters are given as initial capitals when spelled out and as all capitals when abbreviated. For example:

  Prefetch Enable : PE
  Cache Enable : CE

- **Names of Bits and Registers**

  Bit names and register names are presented in initial capitals. For example:

  Host Software Reset
  Sector Count Register

- **Hexadecimal Notation**

  Hexadecimal notation is identified using the small letter form. For example:

  30h

- Signal Negation

  A signal name is defined as active low is listed with a dash character following the signal. For example:

  RD-

- Notes

  Notes are used after tables to provide you with supplementary information.

- Host

  In general, the system in which the drive resides is referred to as the host.

1-4 *Reference*

For additional information about the AT interface, refer to:

- ATA-3 (AT Attachment 3), Revision 7B, 27 January, 1997

Chapter 2
OVERALL DESCRIPTION

This chapter summarizes general functions and key features of Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A drives, as well as the standards and regulations they meet.

2-1 *Introduction*

The Samsung Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A 3.5 inch disk drives are low cost, high capacity, high performance random access devices which use non removable 3.5 inch disk(s) as storage media. The disk is used of thin film metallic media technology for enhanced performance. Each disk surface employs one movable head to access the data tracks. The formatted capacity is 1.27, 2.54, 3.2, 2.16, 1.08, and 2.16 gigabytes of storage, respectively.

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A drives include the AT controller embedded in the disk drive PCB electronics. The drive's electrical interface is compatible with the mandatory, optional and vendor specific commands.

Drive size conforms to the industry standard 3.5 inch form factor. The interface connectors are the standard 40 pin for AT Interface and 4 pin for DC power supplies.

High capacity is achieved by using Advanced Thin Film Inductive head and PRML (Partial Response Maximum Likelihood) recording method. This method can increase capacity by increasing the areal density of the drive..

High performance and low cost are achieved through the use of a rotary voice coil actuator and an embedded servo system. Embedded servo technology uses special information recorded on each data cylinder to maintain position accuracy. This technique assures recording head position accuracy in read or write operations at all temperatures.

The heads, disk and actuator housing is environmentally sealed. Air circulates within the HDA through a non-replaceable recirculating filter to ensure the maintenance of a contamination free disk and actuator environment.

2-2 Key features

Key features of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives include:

- Formatted capacity of 1.27, 2.54, 3.2, 2.16, 1.08, 2.16 Gbytes respectively.
- Low-profile, 1-inch height form factor
- 11 msec average seek time
- High accuracy rotary voice coil actuator with embedded sector servo
- Fast ATA-3 / E-IDE interface
- Power management for "Green PC"
- ATA standard PIO Mode 0-4 / DMA Mode 0-2
- Supports for both CHS and LBA Addressing mode
- Supports for all logical geometries as programmed by the host
- Proprietary 128K read look-ahead cache with a segmented buffer and write stacking capability
- 1:1 interleave on read / write operation
- Transparent media defect mapping
- High performance in-line defective sector skipping
- Automatic error correction and retries
- Optimized 144-bit ECC with triple burst on-the-fly(OTF) correction
- Ability to daisy-chain two drives on the interface
- Automatic magnet latch achieving zero power consumption
- PRML Read channel
- Pseudo Contact Recording, Thin Film Inductive heads

2-3 Standards and regulations

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A depends upon its host equipment to provide proper power and environment to achieve optimum performance and compliance with applicable industry and governmental regulations. Special attention has been given in the areas of safety, power distribution, shielding, audible noise control, and temperature regulation.

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives satisfy the following standards and regulations :

- Underwriters Laboratory (UL) : Standard 1950. Information technology equipment including business equipment.
- Canadian Standards Association (CSA) : Standard C22.2 No.3000-201 Information technology equipment including business equipment.
- Technisher Überwachungs Verein (TÜV) : Standard EN 60 950. Information technology equipment including business equipment.
- CE

2-4 Hardware requirements

Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives are compatible with host computers and controllers that are PC / AT compatible. They are connected to a PC either by:

- Using an adapter board
- Plugging a cable from the drive directly into a PC motherboard with an IDE (Integrated Drive Electronics) interface.

Chapter 3
SPECIFICATIONS

This chapter gives a detailed description of the physical, electrical, and environmental characteristics of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives.

3-1 *Specification Summary*

TABLE 3-1. Specifications

DESCRIPTION	WA31273A / WA32543A / WA33203A	WA31083A / WA32163A	WA32162A
Number of disks	1 / 2 / 3	1 / 2	2
Number of R/W heads	2 / 4 / 5	2 / 4	4
Maximum recording density (BPI)	124,925	107,829	117,598
Maximum flux density (FCI)	140,541	121,308	132,298
Track density (TPI)	6,900		6,000
Data tracks per surface	6,740		5,963
Encoding method	8,9 GCR		
Interface method	Fast ATA-3/E-IDE		
Acturator type	Rotary Voice Coil		
Servo type	Embedded Sector Servo		
Number of Cylinder Reserved	4		
Maximum Data Transfer Rate(Mb/s)	107.9	92.86	86.67
Spindle speed (rpm)	5,400 ± 0.1%		4,500±0.1%

3-2 *Physical Specifications*

TABLE 3-2. Physical specifications

DESCRIPTION	WA31273A / WA32543A / WA33203A / WA32163A / WA31083A	WA32162A
Track pitch (µinches)	154	167
Data head flying height (µinches)	0.8	1.01
Inner most data track radius (inches)	0.8413	0.8291
Outer most data track radius (inches)	1.7841	1.8090
Physical dimensions :		
Length (inches)	5.75	
Width (inches)	4.00	
Height (inches)	1.00	
Weight (lbs)	1.2	

3-3 *Logical Configurations*

TABLE 3-3. Logical configurations

DESCRIPTION	WA31273A WA32543A WA33203A	WA31083A WA32163A	WA32162A
Default logical mode :	2,481	2,094	4,186
Number of cylinders	4,962 6,203	4,190	
Number of heads	16	16	16
Number of sectors	63	63	63

3-4 *Performance Specifications*

TABLE 3-4. Performance specifications

DESCRIPTION	WA31273A WA32543A WA33203A	WA31083A WA32163A	WA32162A
Seek Time (typical) :			
Average seek time	<11 msec		
Track to track seek time	2 msec		
Full stroke seek time	<20 msec		
Data Transfer Rate :			
Maximum to/from media	107.9 Mbits/s	92.86 Mbits/s	86.67 Mbits/s
Maximum to/from buffer	16.6 Mbytes/s	16.6Mbytes/s	16.6Mbytes/s
Average latency	5.6 msec		
Controller overhead	< 0.5 msec		
Rotational Speed	5,400± 0.1% rpm		4500±0.1% rpm
Motor spin up time (Typical)	15 sec		
Motor spin down time (Typical)	7 sec		
Interleave	1 : 1		
Buffer size	128 KBytes		

NOTES : ∗ The seek time is defined as the time for the actuator to seek and settle on the desired track with the drive operating at nominal DC input voltages and nominal operating temperature.

∗ The average seek time is determined by averaging the seek time for 1,000 seeks of random length.

∗ The spin up time is the time elapsed between the supply voltages reaching operating range and the drive being ready to accept all commands.

∗ The controller overhead is the time it takes to start a seek after the drive has been selected.

∗ The average latency time is the time needed for another 1/2 revolution after seek completion.

3-5 *Power Requirements*

TABLE 3-5. Power requirements (EX : WA32543A)

Mode	Typical Current (mA rms)		Typical Power (Watts)	Maximum Power (Watts)
	+5 Volts	+12 Volts		
Spin-up	564	1195	14.4	17.06
Normal Read/Write	477	249	4.92	5.27
Idle	216	225	3.38	3.70
Random Seek	481	521	8.31	8.59
Standby	198	78	1.68	1.91
Sleep	120	78	1.34	1.52

NOTES * Random seek means seek commands with logical random location and 30% duty cycle.

* Random read / write means a combination of random write 256 sectors commands and random read 256 sectors command

3-6 *Environmental Specifications*

TABLE 3-6. Environmental specifications

DESCRIPTION	WA31273A / WA32543A / WA33203A / WA32163A / WA31083A / WA32162A
Ambient Temperature :	
Operating	5~55°C
Non-operating	-40~65°C
Maximum gradient without Condensation	20°C / hr
Relative Humidity : (non-condensing)	
Operation	8~80 %
Non-operation	8~95 %
Maximum wet bulb temperature :	
operating	29 °C
non-operating	40 °C
Altitude (relative to sea level) :	
Operating	-200 to 10,000 ft.
Non-operating	-1,000 to 40,000 ft.
Vibration (1 oct / min sweep sine) :	
Operating	
5-21Hz	0.034"(double amplitude)
22-400Hz	1.5 G (p-p)
Non-operating	
5-21Hz	0.195"(double amplitude)
22-500Hz	8.0 G (p-p)
Shock : (1 / 2 sine pulse, 11ms duration)	
Operation	10 G's
Non-operating	75 G's

TABLE 3-6. Environmental specifications (continued)

DESCRIPTION	WA31273A / WA32543A / WA33203A / WA32163A / WA31083A / WA32162A
Acoustic Noise (Max.Sound Pressure):	
Idle	< 35 dBA
Random Read / Write	< 40 dBA

NOTE : The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives can withstand levels of shock and vibration applied to any of its three mutually perpendicular axes, as in the specifications for shock and vibration. When packed in its shipping container, the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A can withstand a drop from 90cm (5Kg / Box), onto a concrete surface - on any of its six surfaces, three edges, and one corner. The drive can withstand vibration applied to the container of 5-500Hz (p-p), 1.5G.

Chapter 4
INSTALLATION AND OPERATION

This chapter describes how to unpack, mount, configure, and connect the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive. It also describes how to start and operate the drive.

4-1 *Space Requirements*

SAMSUNG ships the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives without a bezel. Figure 4-1 shows the external dimensions of the drive.

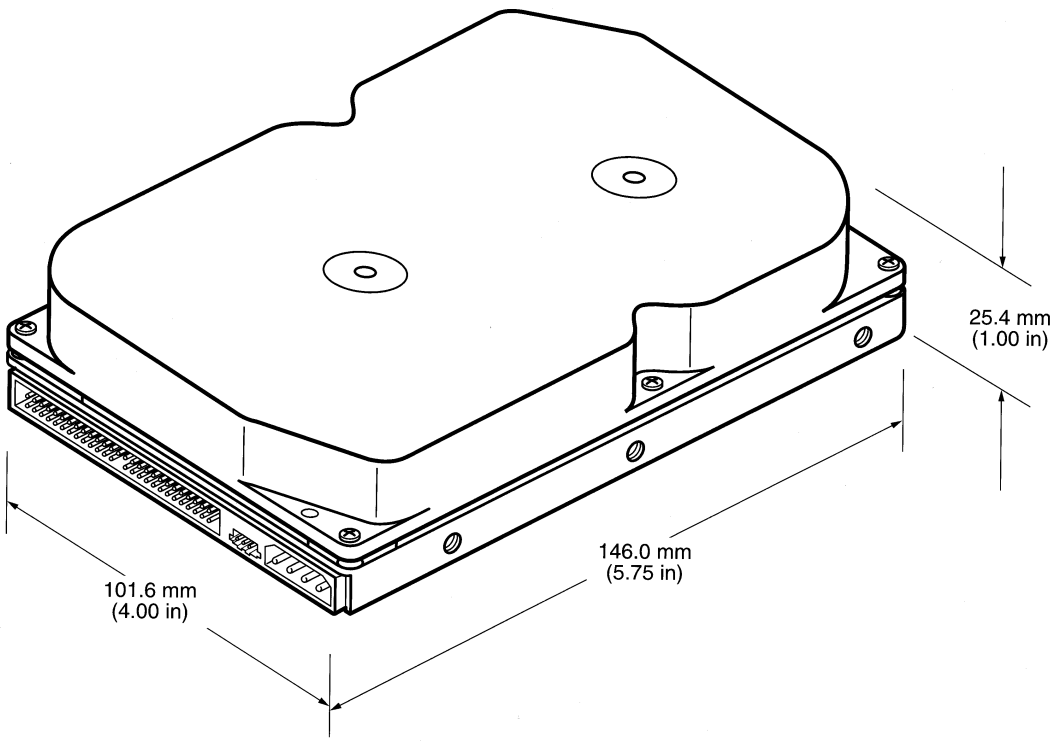


Figure 4-1. Mechanical Dimensions

4-2 *Unpacking Instructions*

(1) Open the shipping container of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A

(2) Lift the packing assembly that contains the drive out of the shipping container.

(3) Remove the drive from the packing assembly. When you are ready to install the drive, remove it from the ESD (Electro Static Discharge) bag.

CAUTION : During shipment and handling the anti static ESD bag prevents electronic component damage due to electrostatic discharge. To avoid accidental damage to the drive, do not use a sharp instrument to open the ESD bag.

(4) Save the packing material for possible future use.

4-3 *Mounting*

(1) Be sure that the system power is off.

(2) Mount the drive in a mounting slot of your system. For mounting, use six #32 UNC screws.

CAUTION : To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 8.0 Kg-cm (6.95 inch-pounds).

4-3-1 Orientation

Figure 4-2 shows the physical dimensions and mounting holes located on each side of the drive. The mounting holes on the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive allow the drive to be mounted in any orientation.

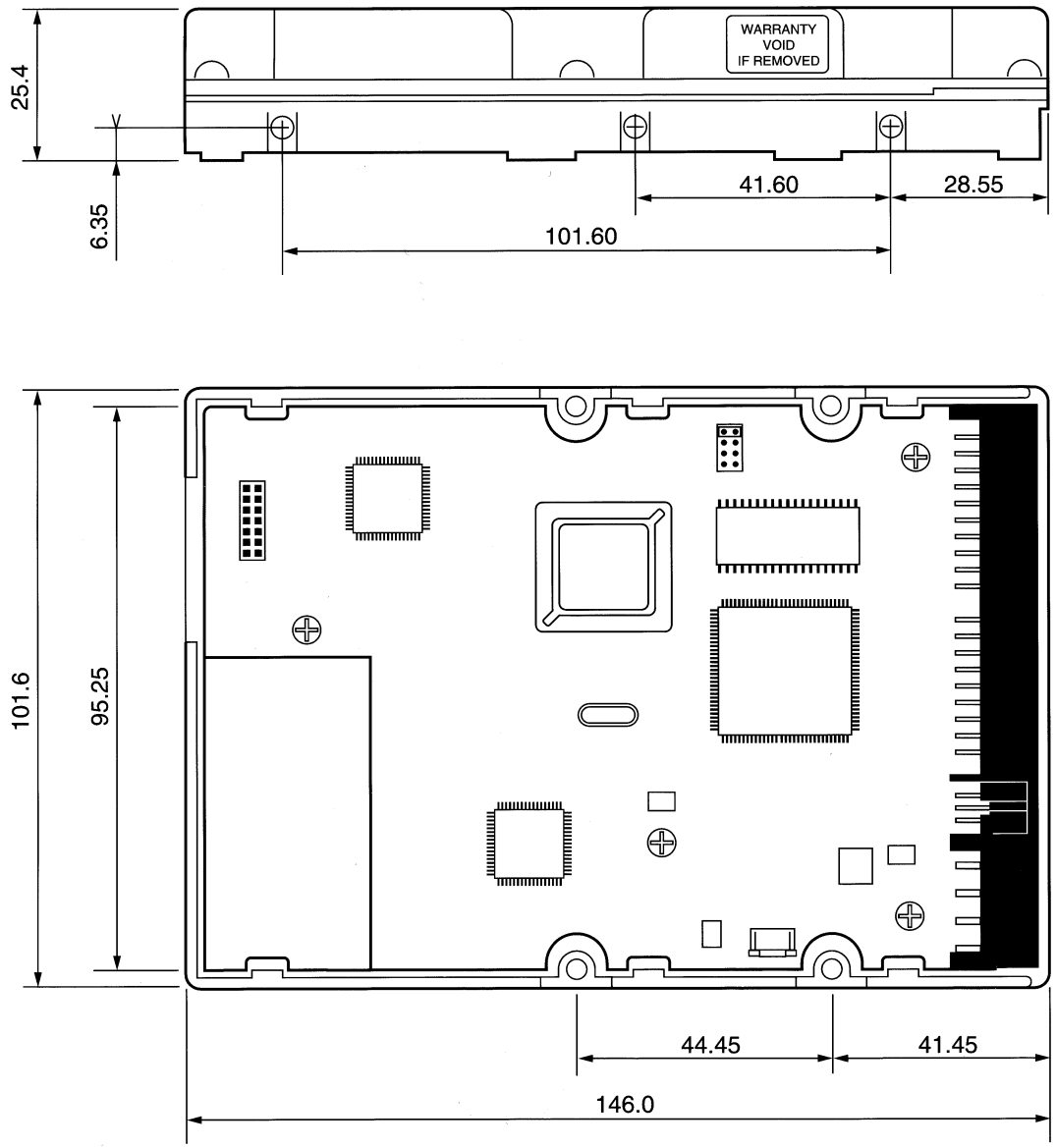


Figure 4-2. Mounting Dimensions (in Millimeters)

4-3-2 Clearance

The printed circuit board (PCB) is very close to the mounting holes. Do not exceed the specified length for the mounting screw described in the Figure 4-3. The specified screw length allows full use of the mounting-hole threads, while avoiding damage or placing unwanted stress on the PCB.

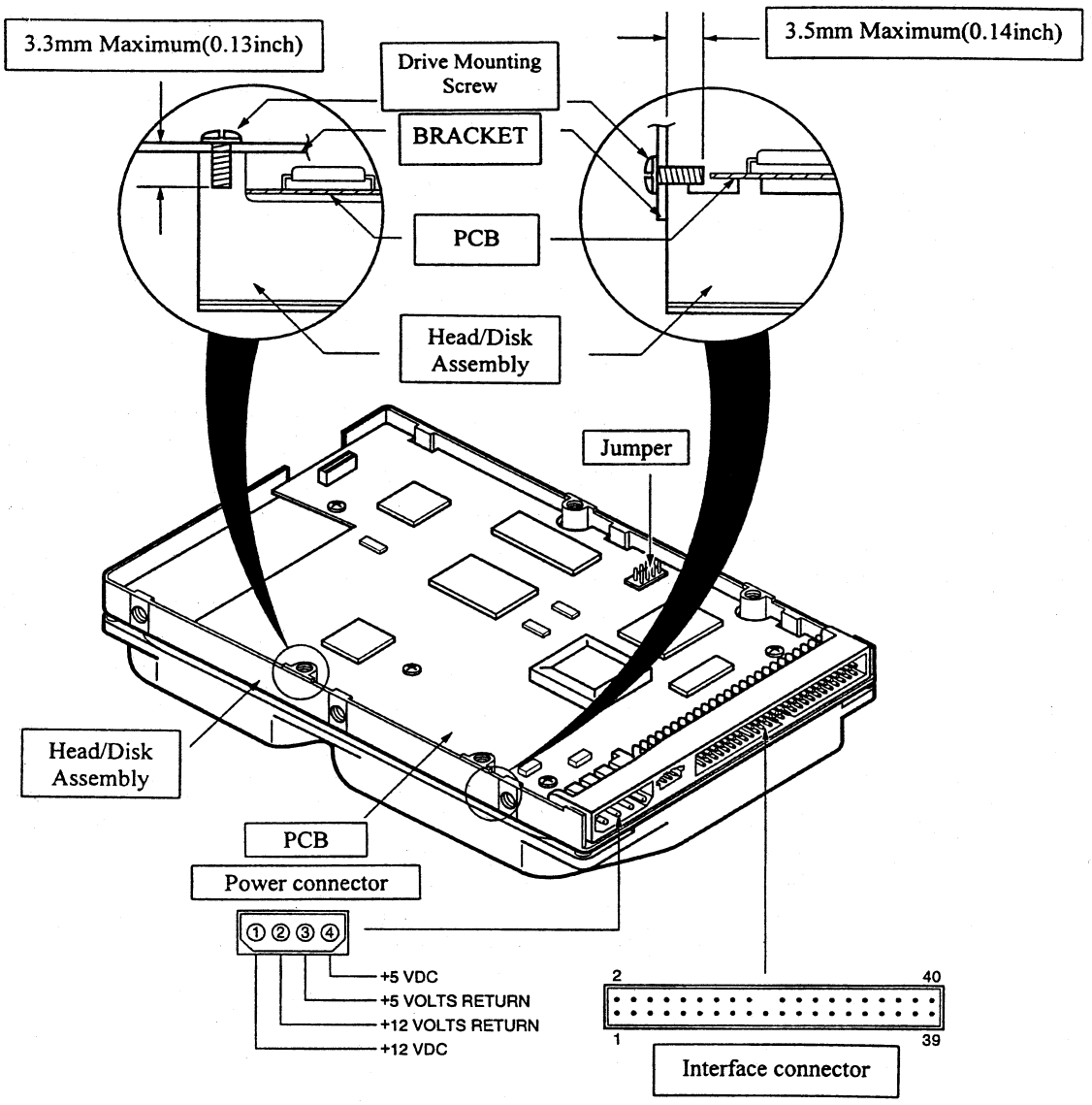


Figure 4-3. Mounting-Screw Clearance

CAUTION : Using mounting screws that are longer than the maximum lengths specified in Figure 4-3 voids the warranty on the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A.

4-3-3 Ventilation

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive operates without a cooling fan, provided the ambient air temperature does not exceed 55°C. Any user-designed cabinet must provide adequate air circulation to prevent exceeding the maximum temperature.

4-4 *Cable Connectors*

4-4-1 DC Power Connector(J7)

The drive's DC power connector (J7) is mounted on the back edge of the Printed Circuit Board (PCB) see to Figure 4-4. Table 4-1 lists the pin assignments.

Table 4-1. Power Connector (J7) Pin Assignment

PIN NUMBER	POWER LINE DESIGNATION
1	+12V DC
2	+12V Return (Ground)
3	+5V Return (Ground)
4	+5V DC

4-4-2 AT-Bus Interface Connector (J2)

The AT-Bus interface connector (J2) on the drive connects the drive to an adapter or an on board AT adapter in the computer. J2 is a 40-pin Universal Header with two rows of 20 pins on 100-mil centers, as shown in Figure 4-4.

To prevent the possibility of incorrectly installing the I/F cable, the connector has been keyed by the removal of Pin #20. The connecting cable is a 40-conductor flat ribbon cable and the maximum cable length is 0.46m (18 inches).

For pin assignments and signal descriptions, see "AT INTERFACE and ATA COMMANDS" in Chapter 6.

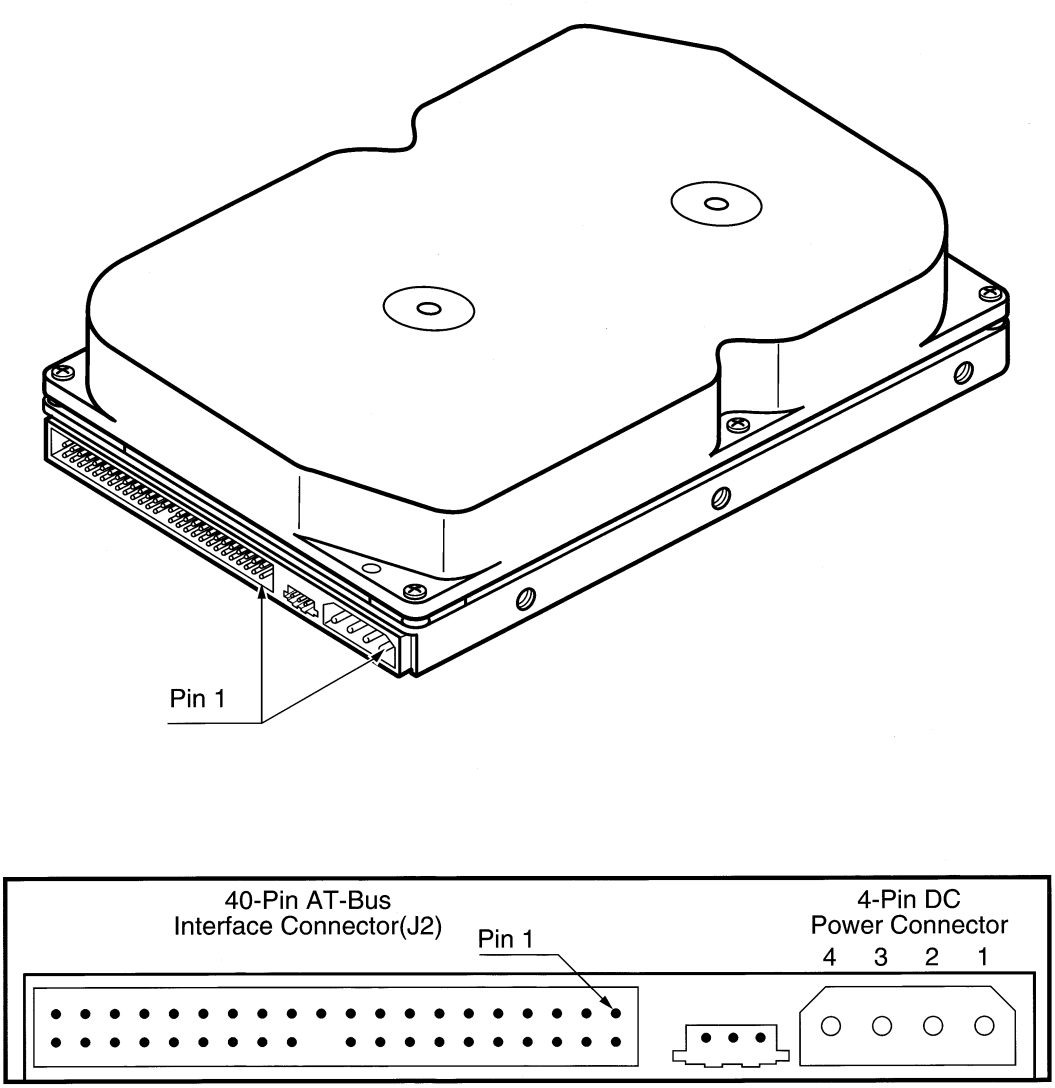
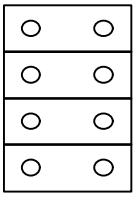


Figure 4-4. DC Power Connector (J7) and AT-Bus Connector (J2)

4-5 *Configuration Jumpers(J5)*

Jumper Definitions:



ST – Reserved for Manufacturing Test Process.

This jumper is used by Samsung engineers for development purpose

CSEL - Cable Select.

This jumper is used if Cable Select line is used for master and slave selection.

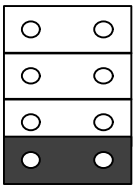
SLAVE - Slave Mode.

This jumper, when installed, is for configuring the drive in Slave Mode. Master jumper must be removed when Slave Mode is configured.

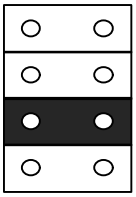
MASTER - Master Mode

This jumper, when installed, is for configuring the drive in Master Mode. This jumper must be removed when drive is configured in Slave Mode

Default Jumper Setting - Master Mode



Slave Jumper Setting - Slave Mode



4-5-1 Master and Slave Jumpers

You can daisy-chain two drives on the AT-Bus interface. When daisy-chaining two drives, specify one drive as the Master, the other as the Slave by combination of master and slave jumpers.

To configure a drive as the Master (Drive 0), install a jumper on the master pins.

Samsung ships the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives from the factory with the master jumper installed (Drive 0), and slave Jumper opened.

To specify a drive as the Slave (Drive) remove the master jumper and install the jumper on the slave pins.

NOTE: The order in which drives are connected in a daisy chain has no significance.

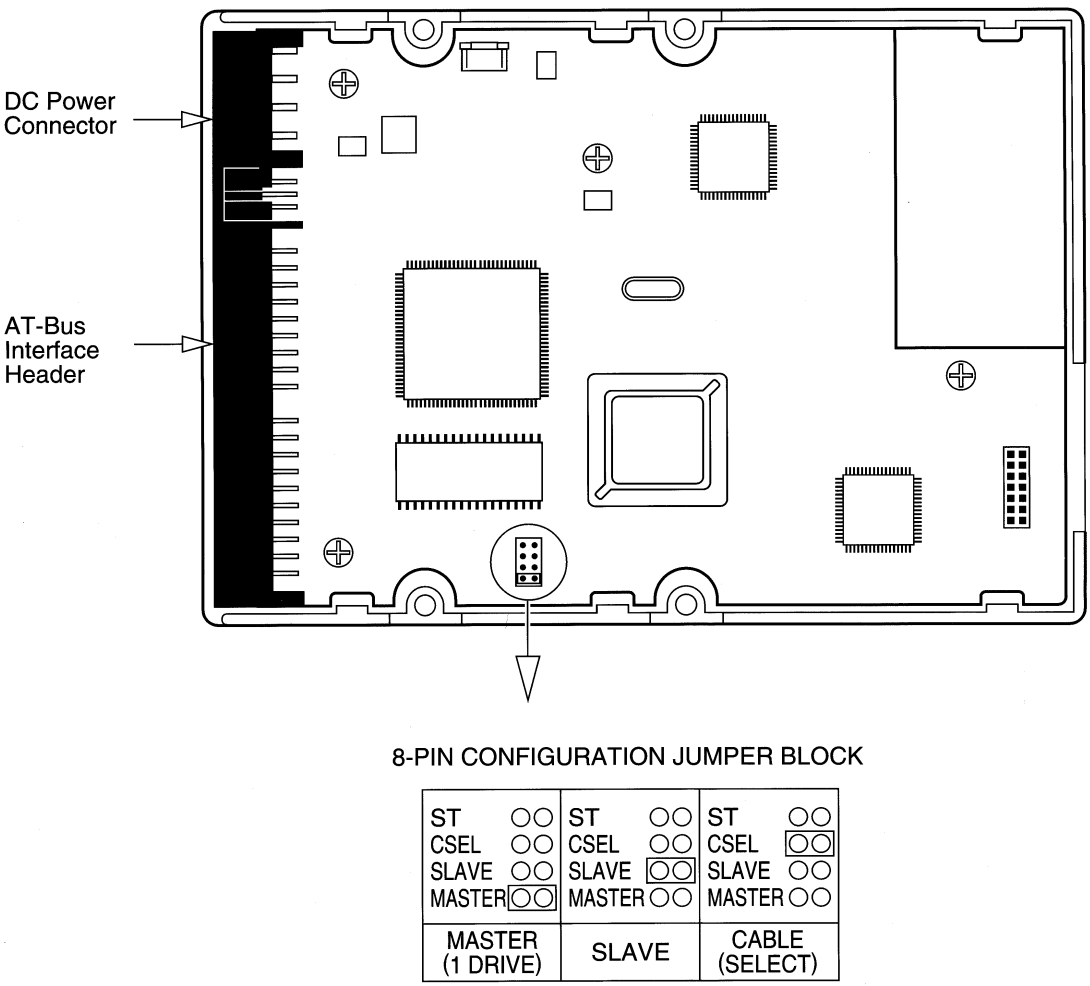


Figure 4-5. Jumper Pin Locations on the Drive PCB

4-5-2 Drive Installation

You can install the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive in an AT-compatible system in two ways.

- To install the drive with a motherboard that contains a 40-pin AT-bus connector, connect the drive to the motherboard using a 40-pin ribbon cable. Ensure that pin 1 of the drive is connected to pin 1 of the motherboard connector.

- To install the drive in a system without a 40-pin, AT-bus connector on its mother board, you need an AT-bus adapter kit. The kit includes an adapter and a ribbon cable, which is used to connect the board to the drive.

NOTE: Removing pin 20 of the drive ensures the connector cannot be installed upside down.

Figure 4-6. indicates the cable and power cable connections required for proper drive installation.

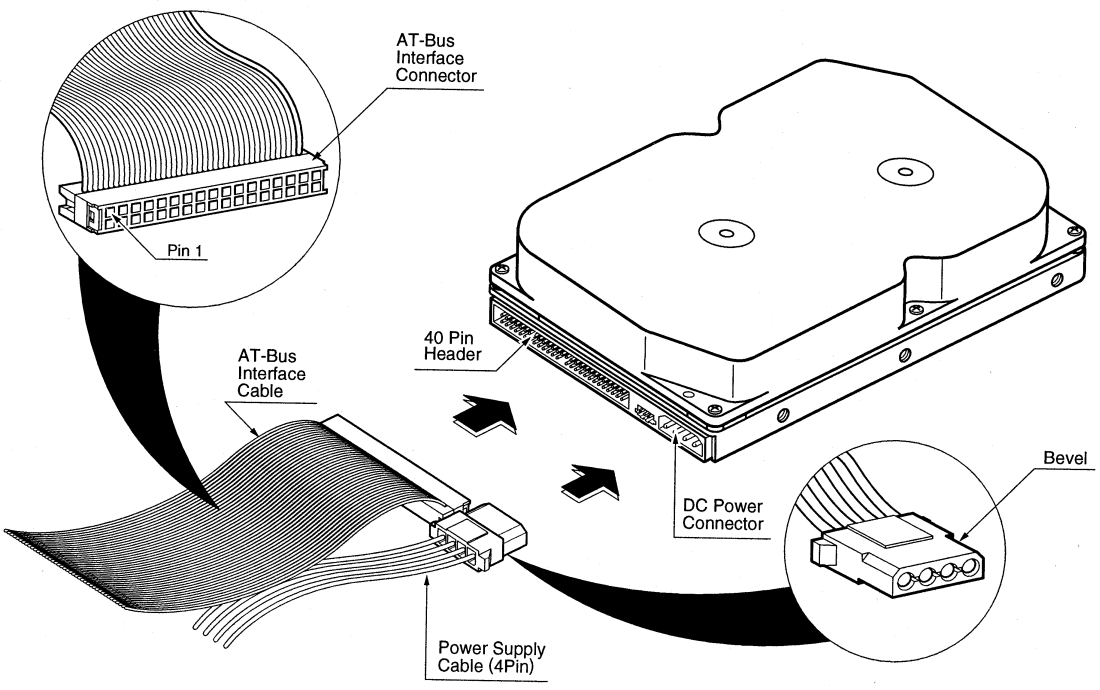


Figure 4-6. DC Power connector and AT-Bus Interface Cable Connections

4-6 *System Startup Procedure*

Once you have installed the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive and the adapter board (if required) in your system, you can to partition and format the drive for operation. To setup the drive correctly, follow these instructions:

(1) Power on the system.

(2) Run the SETUP program. Generally, you will find the SETUP program on a Diagnostics or Utilities disk, or within the system's BIOS (Basic Input Output System).

The SETUP program allows you to enter the types of optional hardware installed - such as the hard disk drive type, the floppy disk drive capacity, and the display adapter type. The system's BIOS uses this information to initialize the system when the power is switched on for instructions on how to use the SETUP program, refer to the system manual for your PC.

(3) Enter the appropriate parameters for the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A

During the AT system CMOS setup, you must enter the drive type for Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A the hard disk drives. This procedure allows the system to recognize the drive by translating its physical drive geometry parameters such as cylinders, heads, and sectors, into a logical addressing mode.

The following table shows the logical parameters that provide the maximum capacity on Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A.

Table 4-3. Logical Drive Parameters

PARAMETER	WA31273A	WA32543A	WA33203A	WA32163A	WA31083A	WA32162A
Logical Cylinders	2480	4962	6202	4190	2094	4186
Logical Heads	16	16	16	16	16	16
Logical Sectors	63	63	63	63	63	63
Total Number Logical Sector	2,499,840	5,001,696	6,251,616	4,223,520	2,110,752	4,219,488
CMOS Setup	1279 MB	2560 MB	3200 MB	2162 MB	1081 MB	2160 MB
Formatted Capacity	1279 MB	2560 MB	3200 MB	2162 MB	1081 MB	2160 MB

If the drive types offered by the CMOS do not support the number of cylinders, heads and sectors shown in the table and your system does not support a "user-defined" drive type, select a drive type whose total number of sectors* are less than or equal to the number of data sectors of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A.

NOTES : * The total numbers of sectors are calculated by (CylindersxHeadsxSectors) of the selected drive type.

See configuration jumper part (4.5) of this manual.

(4) Save the set-up parameters and re-boot the system using the operating system installation disk, for example, MS-DOS, then follow the installation instructions in your operating system manual.

If you are using MS-DOS:

(1) Run the FDISK utility or a third-party partitioning program.

NOTE : When using DOS version 3.2 or below, the DOS partitions only 32 Mbytes of the drive's capacity. DOS 3.3 partitions the drive in multiples of 32 Mbytes. DOS 4.01 or later, or a third-party partitioning program, create partitions that exceed 32 Mbytes.

(2) To format the hard drive and transfer the operating system to the drive, type ;

```
FORMAT C:/S
```

After this command executes, boot the system from the hard drive.

NOTE : A low-level format is not required as this was done at the factory before shipment.

Chapter 5
DISK DRIVE OPERATION

This chapter describes the operation of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A functional subsystems. It is intended as a guide to the operation of the drive, rather than a detailed theory of operation.

5-1 Drive Mechanism

This section describes the mechanism of the drive. the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive consists of a mechanical sub-assembly and a printed circuit board assembly (PCBA) as shown in figure 5-1.

5-1-1 Head Disk Assembly

The head / disk assembly (HDA) contains the mechanical sub-assemblies of the drive, which are sealed between the aluminum-alloy base and cover. The HDA consists of the disk stack assembly, rotary positioner assembly, head stack assembly, actuator latch assembly, and base casting which includes the DC motor assembly. HDA assembly is done in a Class 100 clean room. These subassemblies cannot be adjusted or field repaired.

CAUTION: To avoid contamination in the HDA, never remove or adjust its cover and seals Disassembling the HDA voids your warranty.

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A products are part of a one, two and three disk product family. The Winner 3A WA31273A / WA31083A contains one magnetic disk and two read / write heads and uses both sides of the magnetic disk. The Winner 3A WA32543A / WA32163A, Winner 2A WA32162A have two magnetic disks and four read / write heads, and the Winner 3A WA33203A has three magnetic disks and five read / write heads.

5-1-2 Base Casting Assembly

A one piece, aluminum-alloy base casting provides a mounting surface for the drive mechanisms and PCBA. The base casting also plays the role as the flange for the DC spindle motor assembly. A gasket provides a seal between the base and cover castings that enclose the drive mechanism.

5-1-3 Spindle Motor Assembly

The spindle motor assembly consists of a brushless three-phase motor, spindle bearing assembly, disk mounting hub, and a labyrinth mechanical seal. The entire spindle motor assembly is completely enclosed in the HDA and screwed to the base casting. The labyrinth seal prevents bearing lubricant from coming out into the HDA. The motor rotates the spindle shaft at 5400(Winner 3A) rpm and 4500(Winner 2A) rpm.

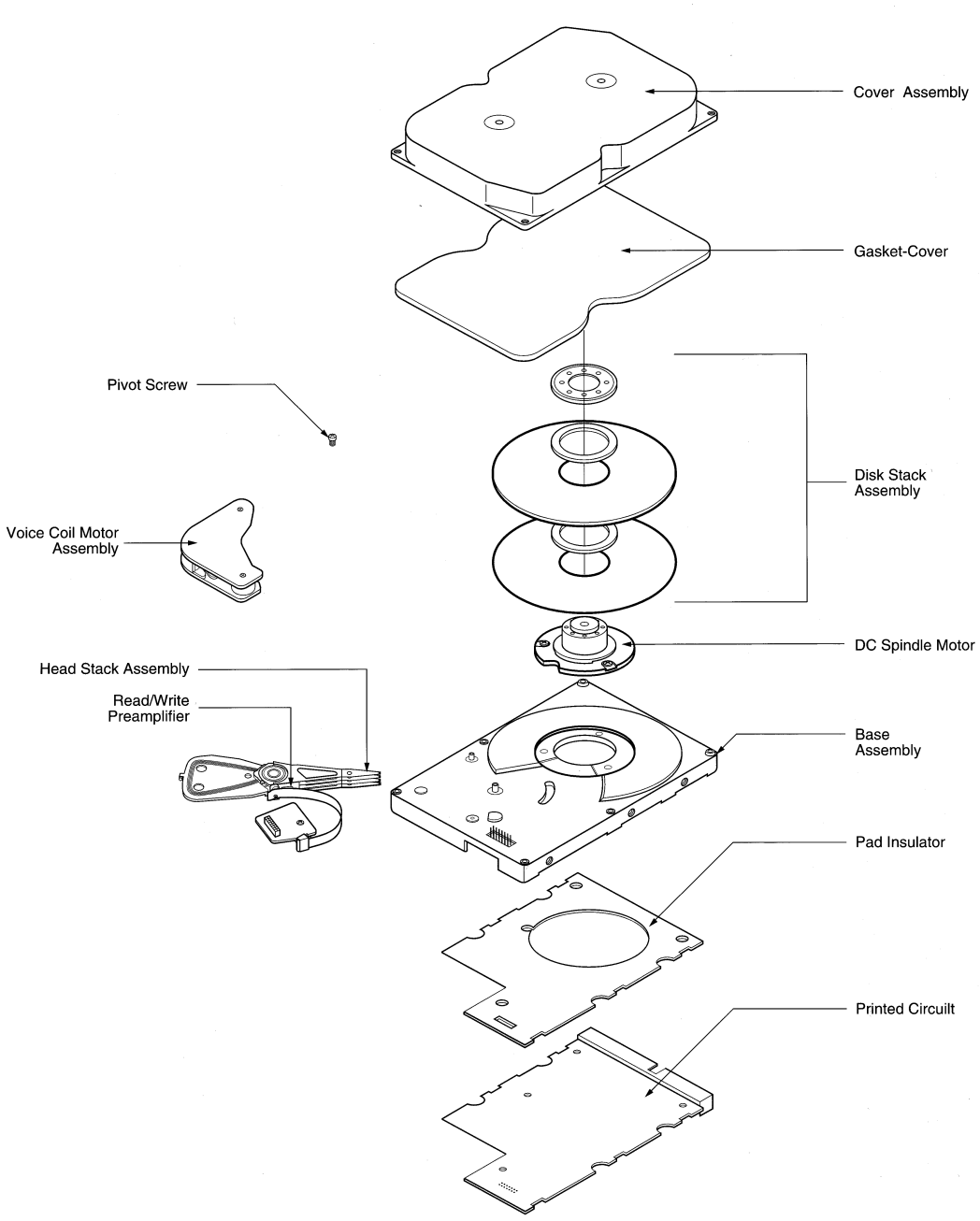


Figure 5-1. Exploded Mechanical view

5-1-4 Disk Stack Assembly

The disk stack assembly in the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drive consists of 1, 2 or 3 disks and disk spacers secured on the hub of the Spindle Motor Assembly by a disk clamp. The aluminum-alloy disks have a sputtered thin-film magnetic coating.

A carbon overcoat protects the disk magnetic surfaces to prevent head and media wear due to head contact with the disk surfaces during head take-off and landing. Head contact with the disk surface occurs only in the landing zone outside of the data area, when the disks are not rotating at full speed. The landing zone is located at the inner diameter of the disk, far beyond the last cylinder of the data area.

5-1-5 Head Stack Assembly

The head stack assembly consists of an actuator / coil sub-assembly, read / write heads, a flexible printed circuit and bearings. The actuator / coil sub-assembly is assembled with actuator and over molded coil. Read / write heads are mounted to spring-stainless steel flexures that are then swage mounted onto the rotary positioning assembly arms of the actuator.

The flexible circuit connects the read / write heads with the PCBA via a connector through the base casting. The flexible circuit contains a read / write Preamplifier IC.

5-1-6 Rotary Positioning Assembly

The rotary positioner, or rotary voice coil motor, is a SAMSUNG proprietary design that consists of upper and lower permanent magnetic yokes fixed to the base casting and a rotary overmolded coil on the head stack assembly. The magnet consists of two alternating poles glued to the magnet yoke. Rubber crash stops mounted on the upper magnet yoke and base casting prevent the head from being flown into the spindle or off of the disk surface.
Current from the power amplifier induces a magnetic field in the voice coil. Fluctuations in the field around the permanent magnets move the voice coil so that heads can be positioned on the requested cylinder.

5-1-7 Air Filtration System

It is very important that air circulating within the drive be free of particles. SAMSUNG HDA's (head/disk assemblies) are assembled in a Class 100 purified air environment to ensure cleanliness. To retain this clean air circulation, the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A is equipped with a recirculating filter, which cleans the air within the HDA. The recirculating filter traps any particles which may be generated during head landing or

take-off. Mounting the recirculating filter close to the disk, positions the filter in the path of the air flow. This strategic placement of the filter allows the rotating disks to act as an air pump forcing air through the recirculating filter.

5-2 Drive Electronics

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A drives attain their intelligence and performance through the specialized electronic components mounted on the PCBA. figure 5-2 shows a simplified block diagram of the the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A electronics. The components are mounted only on one side of the PCBA.

The Preamplifier and Write Driver IC is the only electrical component that is not on the PCBA. It is mounted on the flexible circuit inside the HDA. Locating the Preamplifier IC as close as possible to the read/write heads via surface mount technology improves the signal to noise ratio.

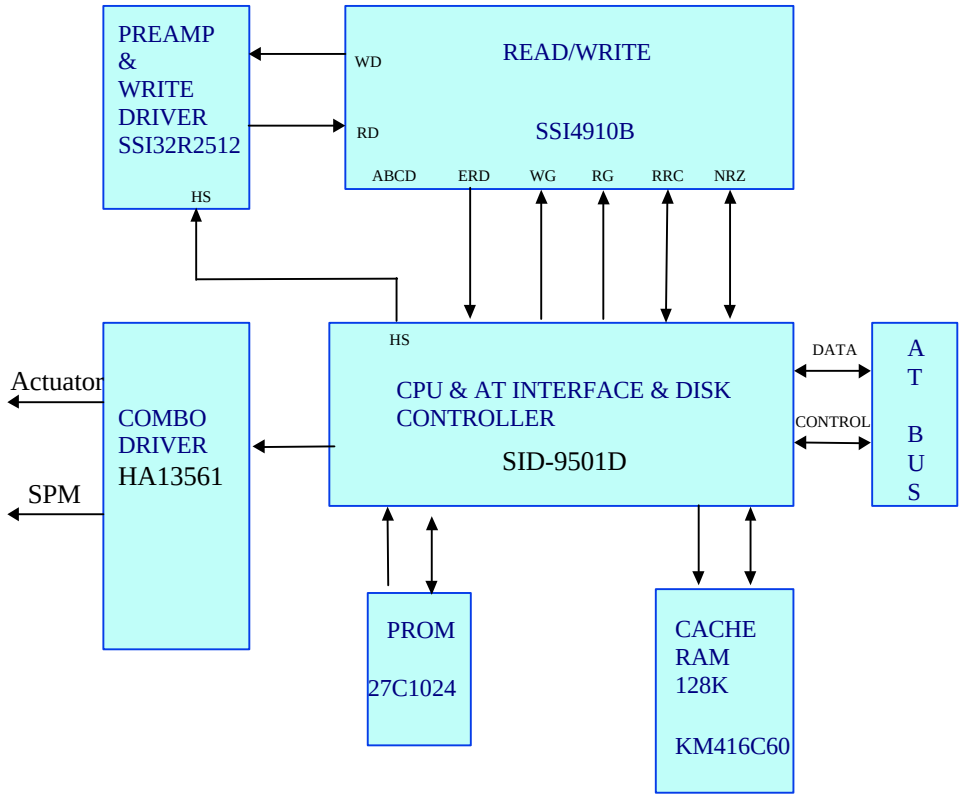


Figure 5-2. ELECTRONICS BLOCK DIAGRAM

5-2-1 Integrated AT Interface, Disk Controller, Buffer Manager and Microprocessor

The Samsung SID-9501 incorporates a high speed 16-bit Fixed Point DSP (PINE Core) microprocessor to perform the ATA interface control, buffer data flow management, disk format/ read/write control, error correction functions of an embedded disk drive controller, as well as embedded servo control. It is through the DSP microprocessor that the SID-9501D communicates to the other control blocks within the device, to the buffer and the disk. The DSP Core provides the following features:

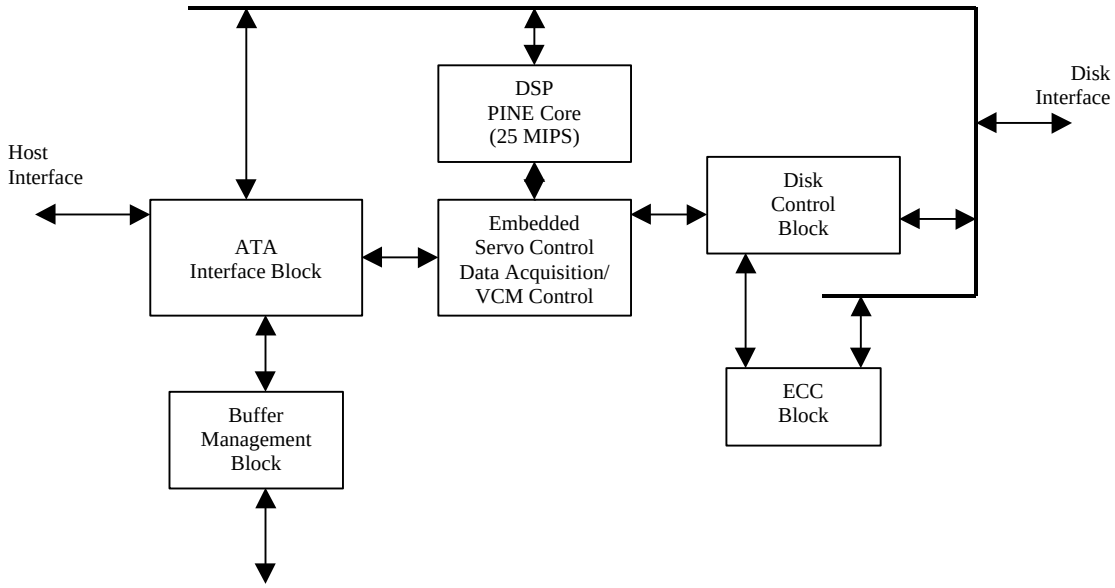
- 40ns cycle time at 5 Volts
- 16-bit Fixed Point DSP (PINE Core)
- 16 x 16bit 2's Complement Parallel Multiplier with 32bit Product
- Single Cycle Multiply and Accumulate
- 36bit ALU with Two 36bit Accumulators
- Programmable DPLL for DSP clock
- On-chip Data RAM (256 word x 2)
- On-chip Program RAM (3K word)

Other Features:

- 5V ± 10% Operation
- Programmable Power-down Modes
- CMOS 0.65μm Standard-cell technology
- 208 pin QFP package

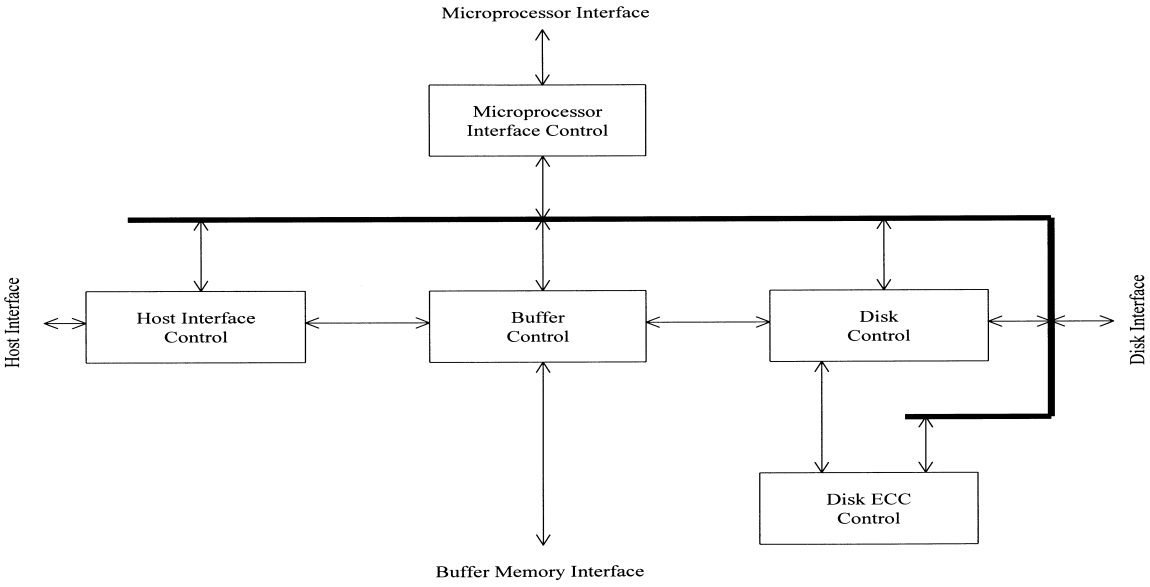
Figure 5-2-1 reveals the various blocks within the SID-9501 along with their generalized interconnection. The blocks described in this figure will be referred to throughout this document.

Figure 5-2-1 SID-9501 Block Diagram



5-2-1-1 ATA Interface Block

The SID-9501D provides an ATA interface to the host computer and can attach to an ATA-1, ATA-2, ATA-3 or ATA-4 host. It provides a means for the host to access the Task File registers used to control the transfer of data between host memory and the disk.



The ATA Host Interface Block can be programmed to execute various host read/write commands either completely automatically without any microprocessor intervention, semi-automatically with minimal microprocessor intervention, or manually with the aid of the microprocessor.

Of particular interest to most designers, are the significant advances in ATA automation which have been incorporated into the SID-9501D. The highlights of ATA automation are:

- Automatic data transfer management for multi-sector Read/Write commands.
- Automatic data transfer management for Read/Write Multiple.
- ATA Multi-word DMA Mode 2 support (16.6MB/sec).
- Fast IDE PIO Mode 4 support (16.6MB/sec).
- Automatic Task File Management.

- Programmable IRQ timer to allow automation to work with different BIOS implementations and different device drivers.
- IORDY for PIO flow control.
- 40-byte host FIFO to allow automation to occur smoothly during discontinuities in transfers on the ATA interface.
- Auto Command support.
- Automation of an extensive portion of the ATA command set.
- LBA or CHS Task File Modes.
- Provides logic for daisy chaingin two embedded disk controllers.
- On-chip 12mA Host Drivers.

The SID-9501D also supports a basic ATAPI environment. this consists of:

- ATAPI Reset command.
- ATAPI Packet command.
- ATAPI Identify Device commands.
- ATAPI Service command.

The SID-9501D supports both PIO and DMA type transfers. The supported DMA type transfers includes single-word, multi-word, and synchronous DMA transfers. DMA transfers and PIO transfers utilize the bus in 8- or 16-bit mode depending upon the command being executed. The bus is automatically switched between 16- and 8-bit mode while performing Read Long and Write Long commands at the time of ECC byte transfers.

Additional functionality is provided in the Host Interface block by the following features:

- Programmable transfer length for automatic ECC byte transfer on the AT bus.
- Automatically inserted wait states are provided to support the IOCHRDY signal pin functions at any ATA interface speed.
- Support for Master/Slave configuration of two embedded disk controller drives.
- Automatic detection of Host status reads.
- Support of both LBA and CHS Task File register formats.
- Automatic detection of both the software AT reset and hardware AT reset.
- 12-mA drivers are provided for direct connection to the ISA/EISA bus. Some ATA inputs are Schmitt trigger inputs.

- Support for PIO modes 0 through 4.
- Support for synchronous DMA transfers.

5-2-1-2 The Buffer Management Block

The Buffer Management block manages the flow of data into and out of the buffer. Significant automation is incorporated which allows buffer activity to take place automatically during read/write operations between the host and the disk. This automation works together with automation within the Host Control and Disk Control blocks to provide more bandwidth for the imbedded DSP microprocessor to perform non-data flow functions. The buffer control circuitry keeps track of buffer full and empty conditions and automatically works with the Disk Control block to stop transfers to or from the disk when necessary. In addition, transfers to or from the host are automatically stopped or started based on buffer full or empty status.

A prioritized five channel port buffer control architecture is implemented (Host, Disk, MPU, ECC and Refresh).

The data path to the buffer RAM is 16-bit path in ATA mode. A parity bit is available for each of the low and high order eight bits.

EDO DRAM support is provided with up to 4 MB addressing capability (Page 8 mode) with up to 50 MB buffer bandwidth.

The buffer Control block incorporates very flexible segmentation support. Two operational segments can be set up to support general read/write, auto write, and read caching (Auto-Read) algorithms. The segment size is programmable to any value up to 4 Mbytes with 2 byte resolution. In addition, there is special segment support for storing disk servo split pointers. The various pointers are designed to automatically wrap at segment boundaries to ensure data integrity without microprocessor intervention.

Additional functionality is provided in the Buffer Management block through the following features:

- Increased automation to support minimal latency read operations with minimal latency and true buffer alignment.
- 16 bits Memory Data Bus.
- Capability to support the execution of multiple consecutive Auto-Write commands without loss of data due to overwriting of data.
- EDO-DRAM support with up to 4 MB addressing capability (Page 8 mode).
- Buffer bandwidth: 50 MB/sec.
- Minimum Latency Read support.
- Auto Data Streaming for Host and Disk.
- Servo Pointer wrap capability.

- Scratch Pad Area Control.
- Read/Write cache support.

5-2-1-3 The Disk Control Block

The SID-9501D Disk Control block manages the flow of data between the disk and the buffer. It is capable of performing completely automated track read and write operations at a maximum data rate of 80 Mbits/sec in dual bit NRZ mode or 160 Mbits/sec in byte wide NRZ mode. Many flexible features and elements of automation have been incorporated to complement the automation contributed by the Host and Buffer blocks.

The Disk Control block consists of the programmable sequencer (Disk Sequencer), automatic CDR/data split field processing, disk FIFO, fault tolerant sync detect logic, and other support logic.

The WCS sequencer contains a 31-by-2 byte programmable SRAM and associated control logic, which is programmed by the user, to automatically control all single track format, read, and write operations. From within the sequencer micro program, the Disk Control block can automatically deal with such real time functions as defect skipping, servo burst data splitting, branching on critical buffer status, address verification, and data compare operations. Once the Disk Sequencer is started, it executes each word in logical order. At the completion of the current instruction word, it either continues to the next instruction, continues to execute some other instruction based upon an internal or external condition having been met, or stops. During instruction execution or while stopped, registers can be accessed by the embedded microprocessor to obtain status information reflecting the Disk Sequencer operations taking place.

In addition to the flexible Disk Sequencer, the Disk control block contains many other features which are available to satisfy diverse requirements. These include:

- Support for optimized zero latency read operations.
- Disk Transfer Length register monitoring in Disk Sequencer.
- Support for Headerless Format.
- 160 Mbps 8 bits / 80 Mbps Dual bit NRZ Data Processing.
- Index counter for power management command support.
- Embedded Servo Field Skipping.
- Automatic time-out support when waiting for Sync, Index, Sector, and End of Servo burst to relieve microprocessor of overhead associated with managing time outs.
- 34 Byte Disk FIFO.
- Automatic Split Field Processing for CDR.
- Automatic timeout with two-revolution timer

- Automatic timeout on the Sync Field..
- A 34-byte FIFO between the buffer and the Disk Control block smoothes out data flow attributed to discontinuities in data or differences in speed.
- Defect Management with skip flag..
- PRML read channel support.
- Automatic internal Sector Mark generation (no external Sector Mark needed).
- Automatic Sector/Servo Mark alignment.

5-2-1-4 The Disk ECC Block

The SID-9501D provides 3-way interleaved 144 bit Reed-Solomon ECC On The Fly correction. The code is capable of correcting up to three bursts per interleave in hardware. The Disk ECC block also supports 4 bytes bits of CRC data to the ECC generator to allow for greater data integrity in a headerless environment

Error detection and correction is handled in the Disk Control block. Automatic on-the-fly hardware correction will take place for up to three symbols in error per interleave. Correction is guaranteed to complete before the ECC Field of the sector following the sector where the error occurred utilizing standard ATA size sectors. Optional burst limiting can be used to decrease the probability on misdetection and miscorrection.

5-2-1-5 Data Acquisition / VCM / Embedded Servo Control

The SID-9501D provides control for Data Acquisition, VCM control and support of Embedded Servo. Features include:

- 10-bit resolution, 3-step Flash AD converter.
- 5 Channels of Analog Data Input
- 1.2µs conversion time per channel
- Pipelined Conversion Mode
- 12-bit resolution DAC
- Programmable Servo Address Mark control
- Di-pulse Gray Code decoder
- Programmable read channel interface

5-2-2 Read/Write IC

The Read/Write IC, shown in figure 5-4, provides read/write processing functions for the drive. The Read/Write IC receives the RD GATE and WR GATE signals, write data, and servo AGC and gates from the Interface Controller. the Read/Write IC sends decoded read data and the read reference clock. It receives write data from the Interface Controller.

When it is connected to the output of the head amplifier it performs the signal conditioning, data qualification, data synchronization and encoding/decoding task with a minimum of external components. There are 5 major functional modules in the Read/Write IC:

- Automatic Gain Control (AGC)
- Filter/Equalizer
- Pulse Qualifier
- Data Separator
- Servo Demodulator

These modules are described in the following sections and shown in figure 5-2-2

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5-2-2-1 Automatic Gain Control (AGC)

The Automatic Gain Control (AGC) is used to maintain a constant signal amplitude at the input of the pulse detector while the input to the amplifier varies.

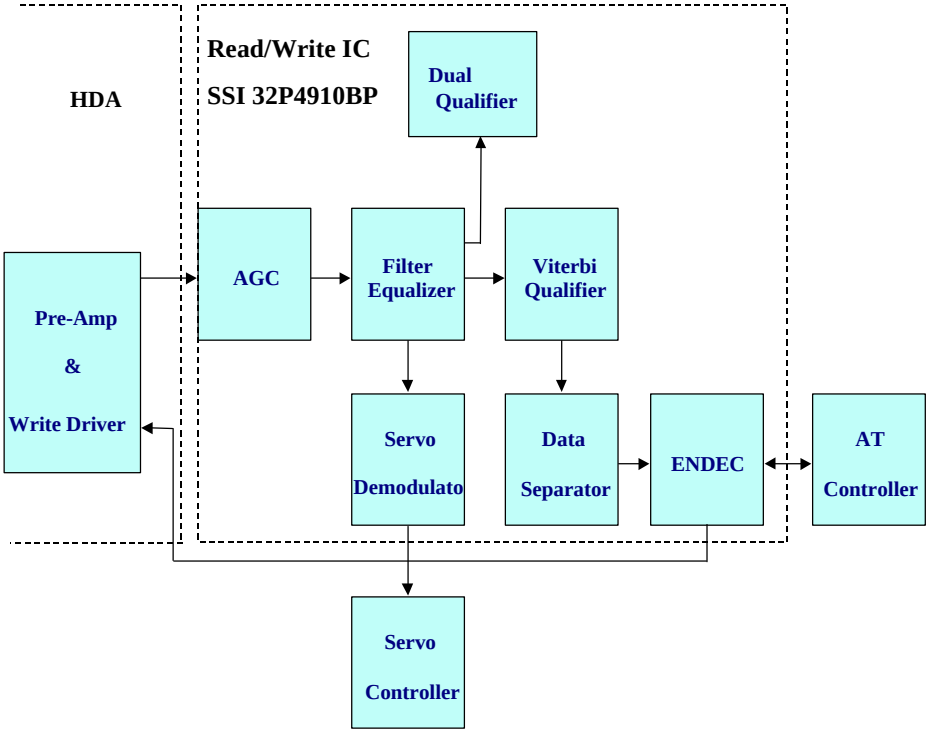

Figure 5-2. Read/Write (SSi32P4910BP) Block Diagram

5-2-2-2 Filter/Equalizer

The filter section provides low pass filtering, boost, and differentiation. Equalizer is used for the fine shaping of the incoming read signal to the PR4 wave shape up to 7dB.

5-2-2-3 Pulse Qualifier

During servo reads this qualifier provides the qualified servo pulse and the polarity of the pulse. During data reads this qualifier is used for ensuring pulse polarity changes during VCO sync field counting.

The viterbi qualifier is only used during data read mode after the sync field count has been achieved. This qualifier has two significant blocks, one that feeds the other. The first block is the sampled pulse detector, it performs the pulse acquisition/detection in the sampled domain. It acquires pulses by comparing the code clock sampled level of the analog waveform to the positive and negative thresholds established by the programmable viterbi threshold window. After the pulses have been detected they must be further qualified by the survival sequence registers and associated logic.

5-2-2-2 Data Separator

The data separator provides complete encoding, decoding, and synchronization for 8,9(0,4,4) GCR data. In data read mode, this circuit performs clock recovery, code word synchronization, decoding, sync byte detection, de-scrambling, and NRZ interface conversation.

5-2-3 Servo Demodulator

The servo demodulator captures four separate servo bursts and provides an amplified and offset version of the voltages captured for each at the A, B, C and D output.

5-2-3 Preamplifier and Write Drive IC

The Preamplifier and Write Drive IC provides the R/W head selection, preamplifier and write driver functions. It amplifies the low-amplitude single ended ΔI current the R/W heads generate and transmits them to the Pulse Detector module in the Read/Write IC. It also outputs the write data receives from the Read/Write IC.

5-3 Servo System

The Servo System controls the position of the read/write heads and holds them on track during read/write operations. The Servo System also compensates for thermal offsets between heads on different surfaces and vibration and shock applied to the drive.

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A is an Embedded Sector Servo System Positioning information is radially located in 72 evenly-spaced servo sectors on each track.

Radial position information can be provided from these sectors for each data head, 72 times per revolution. Because the drive used multiple data zones and each zone has a different bit density, split data fields are necessary to optimally use the non-servo area of the disk. The servo area remains phase-coherent across the surface of the disk, even though the disk has various data zones. The main advantage of the Embedded Sector Servo System is that it can eliminate the problems of static and dynamic offsets between heads on different surfaces. The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A Servo System is classified as a digital servo system because the track-following control and seek control, bias cancellation, and other typical tasks are done in SID-9501D DSP microprocessor.

The Servo system has three modes of operation, track-following mode, settle mode, velocity control mode.

1. The track-following mode is used when heads are “on-track.” this is a position loop with an integrator in the compensation.

2. The Settle mode is used for all access; head switches, short-track seeks and long-track seeks. The settle mode is a position loop with velocity damping. The settle mode does not use feed forward.

3. The velocity control mode is used for acceleration and deceleration of the actuator for two or

more track seeks. The seek operation of this length is accomplished with a velocity control loop. The drives ROM stores the velocity profile in look-up table.

The feed forward compensation is used while the bandwidth of the control loop is kept low.

5-4 Read and Write Operations

The following two sections describe the read channel and write channel operations.

5-4-1 The Read Channel

The drive has one read/write head for each of the data surfaces. The signal path for the read channel starts at the read/write heads. When the magnetic flux transitions recorded on a disk pass under the head, they generate low-amplitude, differential output voltages. The read/write head transfers these signals to the flexible circuit's preamplifier, which amplifies the signal.

The flexible circuit transmits the preamplified signal from the HDA to the PCBA. The PRML channel on the PCBA shapes, filters, detects, synchronizes and decodes the data from the disk. The Read/Write IC then sends the resynchronized data output to the SID-9501D (Disk Controller block).

The SID-9501D Disk Controller block manages the flow of data between the Data Synchronizer on the Read/Write IC and its AT Interface Controller. It also controls data access for the external RAM butter. The ENDEC of SSI32P4910BP decodes the 8,9 GCR format to give a serial bit stream. This NRZ (Non Return to Zero) serial data is converted to 8-bit bytes.

The Sequencer module identifies the data as belonging to the target sector. After a full sector is read, the SID-9501D checks to see if the firmware needs to apply an ECC algorithm to the data. The buffer Controller section of the SID-9501D stores the data in the cache and transmits the data to the AT bus.

5-4-2 The Write Channel

The signal path for the write channel follows the reverse order of that for the read channel. The host transmits data via the AT bus to the SID-9501D Interface Controller block. The Buffer Management block of the SID-9501D stores the data in the cache. Because the data is transmitted to the drive at a rate that exceeds the rate at which the drive can write data to the disk, data is stored temporarily in the cache. Thus, the host can present data to the drive at a rate independent of the rate at which the drive can write data to the disk.

Upon correct identification of the target address, the data is shifted to the Sequencer which generates and appends an error correcting code. The Sequencer then converts the bytes of data to a serial bit stream. The AT controller also generates a preamble field, inserts an address mark, and transmits the data to the ENDEC in the R/W IC where the data is encoded into the 8,9 GCR format and precompensates for non-linear transition shift. The amount of write current is set by 3 GPIO signals that come from the SID-9501D integrated controller chip.

The SID-9501D switches the Preamplifier and Write Driver IC to write mode and selects a head. Once the Preamplifier and Write Driver IC receives a write gate signal, it transmits current reversals to the head, which writes magnetic transitions on the disk

5-5 Firmware Features

This section describes the firmware features as follows:

- Read Cache
- Write Cache
- Write Auto Reassign
- Defect Management
- Power Management
- Triple burst ECC Correction
- SMART (Self-monitoring and reporting technology)

5-5-1 Read Caching

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives use a 128K Read Cache to enhance drive performance. The feature significantly improves system throughput. Use the SET FEATURES command to enable or disable Read Caching. Read caching anticipates host-system requests for data and stores that data for faster future access. When the host requests a certain segment of data, the cache feature uses a prefetch strategy to get the data in advance and automatically read and store the following data from the disk into fast RAM. If the host requests this following data, the RAM is accessed rather than the disk.

There is a high probability that subsequent data requested will be in the cache, because more than 50 percent of all disk requests are sequential. It takes microseconds rather than milliseconds to retrieve this cached data. Thus Read Caching can provide substantial performance improvements during at least half of all disk requests. For example, Read Caching could save most of the disk transaction time by eliminating the seek and rotational latency delays that prominently dominate the typical disk transaction.

Read Caching operates by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a non-caching controller, the SID-9501D interface Controller block continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache memory.

The cache memory consists of a 128K SRAM buffer allocated to hold the data. This cache memory can be directly accessed by the host by means of read and write commands. The unit of data stored is the logical block, or a multiple of the 512-byte sector. Therefore, all accesses to cache memory must be in multiples of the sector size. The following commands empty the cache:

- IDENTIFY DRIVE (ECh)
- FORMAT TRACK (50h)

- EXECUTE DRIVE DIAGNOSTIC (90h)
- READ LONG (23h)
- WRITE VERIFY (3Ch)
- INITIALIZE DEVICE PARAMETER (91h)
- SLEEP (99h, E6h)
- STANDBY IMMEDIATELY (94h,E0h)
- READ BUFFER (E4h)
- WRITE BUFFER (E8h)
- WRITE SAME (E9h)

5-5-2 Write Caching

Write caching improves both single and multi-sector write performance by reducing delays introduced by rotational latency. When the drive writes a pattern of multiple sequential data, it stores the data to a cache buffer and immediately sends COMMAND COMPLETE message to the host before it writes the data to the disk.

The data is then written collectively to the drive thereby minimizing the disk seeking operation. Data is held in cache no longer than the maximum seek time plus rotational latency. Host retries must be enabled for write cache to be active.

If the data request is random, the data of the previous command is written to the disk before COMMAND COMPLETE is posted for the current command. Read commands work similarly. The previous write is allowed to finish before the read operation starts.

If a defective sector is found during a write, that sector is automatically relocated before the write occurs. This ensures that cached data that already has been reported as written successfully gets written, even if an error should occur.

If the sector is not automatically relocated, the drive drops out of write caching and report the error as an ID Not Found. If the write command is still active on the AT interface, the error is reported during that command. Otherwise, it is reported on the next command.

5-5-3 Defect Management

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A media is scanned for defects as part of the factory test process. After the defect scanning the defective sectors are saved in the defect list. The defect encountered in manufacturing process is slipped to next physical sector location. All logical sector numbers are pushed down to maintain sequential order of data. The read/write operation can “slip” over the defective sectors and performance impact is idle time during defective sectors only.

The defect list contains two different tables, the first is data defective sectors and servo defective sectors. The second is S-list, S-list is created to speed up the search for the R-list, it is used as the look up table for the R-list.

5-5-4 Write Auto Reassign

The automatic defect allocation feature automatically maps out defective sectors identified during execution of a write command. If drive gets write error during accessing data sector and error recovery sequence can not recover the error, data sectors which are in that servo frame reassigned. Features:

- Support up to 50 sectors (expandable up to 114 sectors)
- Use binary search method to minimize overhead
- Capability to reassign not only write errors, but also read errors available.
- Use more scratch pad to save variables during auto reassignment to minimize use of internal memory.

Basic Operation:

- Use all unused spare sectors of each zone for reassign
- Reserve ½ track of each spare cylinder for auto reassign
- Reassign List Table is initialized at the end of defect free process in factory test process
- Reassign List Table Location
    - Disk: Cyl-0, Head-2,3, Sector-50-51
    - Buffer: 0x2A00 ~ 0x2BFF (0x2DFF)
- Scanning the Defect List includes scanning the Reassign List includes scanning the Reassign List during normal read/write operation.
- Auto Reassign is done only by updating the Reassign List

5-5-5 Multi-burst ECC Correction

The drive uses a 144 bit Reed-Solomon code to perform error detection and correction. For each 512 byte block, the software error correction polynomial is capable of correcting:

- one single burst error
- three burst error

Single bursts of 65 bits or less and three 17 bit burst error or less are corrected on the fly with no performance degradation.

5-5-6 SMART

The Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A supports SMART (Self-Monitoring, Analysis and Reporting Technology). The following commands are featured:

- SAAS: Disable/Enable (0/1) Attribute Auto Save
- SDSO: Disable SMART operation
- SESO: Enable SMART operation
- SISV: Initialize SMART variables
- SRAT: Read Attribute values
- SRSS: Return SMART status
- SSAV: Save Attribute Values

Chapter 6
AT INTERFACE and ATA COMMANDS

6-1 *Introduction*

A SAMSUNG Disk Drive with an Embedded AT Interface fully supports and enhances the PC mass storage requirements. The SAMSUNG AT interface conforms to the ANSI CAM (X3T9.2) standards in Cabling, in Physical Signals, and in Logical Programming schemes. The SAMSUNG Embedded AT controller joins the industry premiere VLSI circuitry with ingenious programming skill that does not compromise performance or reliability. SAMSUNG integrates and delivers the cutting edge in technology. SAMSUNG AT class disk drives are designed to relieve and to enhance the I/O request processing function of system drivers.

6-2 *Physical Interface*

6-2-1 Signal Conventions

Signal names are shown in all upper case letters. Signals can be asserted (active, true) either a high (more positive voltage) or low (less positive voltage) state. A dash character (-) at the beginning or end of a signal name indicates that it is asserted at the low level (active low). No dash or a plus character (+) at the beginning or end of a signal name indicates it is asserted high (active high). An asserted signal may be driven high or low by an active circuit, or it may be allowed to be pulled to the correct state by the bias circuitry.

Control signals that are asserted for one function when high and asserted for another function when low are named with the asserted high function name followed by a slash character (/), and the asserted low function name followed with a dash (-), e.g. BITENA/BITCLR- enables a bit when high and clears a bit when low. All signals are TTL compatible unless otherwise noted. Negated means that the signal is driven by an active circuit to the state opposite to the asserted state (inactive, or false) or may be simply released (in which case the bias circuitry pulls it inactive, or false), at the option of the implementor.

6-2-2 Signal Summary

The physical interface consists of single ended TTL compatible receivers and drivers communicating through a 40-conductor flat ribbon non-shielded cable using an asynchronous interface protocol. The pin numbers and signal names are shown in Table 6-1. Reserved signals are be left unconnected. 6-2-3 Signal Descriptions

6-2-3 Signal Descriptions

The interface signals and pins are described below in more detail than shown in Table 6-1. The signals are listed according to function, rather than in numerical connector pin order.

6-2-3-1 CS1FX- (Drive Chip Select 0)

This is the chip select signal decoded from the host address bus used to select the Command Block Registers.

6-2-3-2 CS3FX- (Drive Chip Select 1)

This is the chip select signal decoded from the host address bus used to select the Control Block Registers.

6-2-3-3 DA0-2 (Drive Address Bus)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.

6-2-3-4 DASP- (Drive Active/Slave Present)

This is a time-multiplexed signal that indicates that a drive is active, or that Drive 1 is present. This signal is an open collector output and each drive has a 10K ohm pull-up resistor on this signal.

During power on initialization or after RESET- is negated, DASP- is asserted by Drive 1 within 400 msec to indicate that Drive 1 is present. Drive 0 allows up to 450 msec for Drive 1 to assert DASP-. If Drive 1 is not present, Drive 0 may assert DASP- to drive an activity LED. DASP- is negated following acceptance of the first valid command by Drive 1 or after 31 seconds, whichever comes first. Any time after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

6-2-3-5 DD0-DD15 (Drive Data Bus)

This is an 8- or 16-bit bi-directional data bus between the host and the drive. The lower 8 bits are used for 8-bit transfers e.g. registers, ECC bytes.

6-2-3-6 DIOR- (Drive I/O Read)

This is the Read strobe signal. The falling edge of DIOR- enables data from a register or the data port of the drive onto the host data bus, DD0-DD7 or DD0-DD15. The rising edge of DIOR- latches data at the host.

6-2-3-7 DIOW- (Drive I/O Write)

This is the Write strobe signal. The rising edge of DIOW- clocks data from the host data bus, DD0-DD7 or DD0- DD15, into a register or the data port of the drive.

6-2-3-8 DMACK- (DMA Acknowledge)

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

6-2-3-9 DMARQ (DMA Request)

This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. The signal is used in handshake manner with DMACK- (i.e. the drive shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer).

When a DMA operation is enabled, IOCS16-, CSIFX- shall not be asserted and transfers shall be 16-bits wide.

6-2-3-10 INTRQ (Drive Interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control Register. If nIEN=1, or the drive is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

INTRQ is negated by:

- assertion of RESET- or
- the setting of SRST of the Device Control Register or
- the host writing to the Command Register or
- the host reading from the Status Register

On PIO transfers, INTRQ is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the Set Multiple command. An exception occurs on Format Track, Write Sector(s), Write Buffer and Write Long commands - INTRQ shall not be asserted at the beginning of the first data block to be transferred.

6-2-3-11 IOCS16- (Drive 16-bit I/O)

IOCS16- indicates to the host system that the 16-bit data port has been addressed and that the drive is ready to send or receive a 16-bit word. This is an open collector output.

- When transferring in PIO mode, if IOCS16- is not asserted, DD0-7 are used for 8-bit transfers.
- When transferring in PIO mode, if IOCS16- is asserted, DD0-15 are used for 16-bit data transfers.

6-2-3-12 IORDY (I/O Channel Ready)

This signal is active low to extend the host transfer cycle of any host register access (Read or Write) when the drive is not ready to respond to a data transfer request. When IORDY is not negated, this signal is in the high impedance state.

6-2-3-13 PDIAG- (Passed Diagnostics)

This signal is asserted by Drive 1 to indicate to Drive 0 that it has completed diagnostics. A 10K pull-up resistor is used on this signal by each drive.

Following a power on reset, software reset or RESET-, Drive 1 negates PDIAG- within 1 msec (to indicate to Drive 0 that it is busy). Drive 1 then asserts PDIAG- within 30 seconds to indicate that it is no longer busy, and is able to provide status. After the assertion of PDIAG-, Drive 1 will be unable to accept commands until it has finished its reset procedure and is Ready (DRDY=1).

Following the receipt of a valid Execute Drive Diagnostics command, Drive 1 negates PDIAG- within 1 msec to indicate to Drive 0 that it is busy and has not yet passed its drive diagnostics. If Drive 1 is present then Drive 0 waits for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for Drive 1 to assert PDIAG-. Drive 1 clears BSY before asserting PDIAG-, as PDIAG- is used to indicate that Drive 1 has passed its diagnostics and is ready to post status.

If DASP- was not asserted by Drive 1 during reset initialization, Drive 0 posts its own status immediately after it completes diagnostics, and clears the Drive 1 Status Register to 00h. Drive 0 will be unable to accept commands until it has finished its reset procedure and is Ready (DRDY=1).

6-2-3-14 RESET- (Drive Reset)

This signal is asserted from the host system to reset the drive. It shall be asserted for at least 25 µsec after voltage levels have stabilized during power on and negated thereafter unless some event requires that the drive(s) be reset following power on.

Table 6-1 shows the correlation between the signals at the ATA interface and the host AT bus.

Table 6-1. AT-Bus Interface Signals

Drive Connector		Direction	AT System BUS
Signal Name	Pin No.		
RESET-	1	←—	RESET DRV
Ground	2	——	Ground
DB7	3	←→	SD7
DB8	4	←→	SD8
DB6	5	←→	SD6
DB9	6	←→	SD9
DB5	7	←→	SD5
DB10	8	←→	SD10
DB4	9	←→	SD4
DB11	10	←→	SD11
DB3	11	←→	SD3
DB12	12	←→	SD12
DB2	13	←→	SD2
DB13	14	←→	SD13
DB1	15	←→	SD1
DB14	16	←→	SD14
DB0	17	←→	SD0
DB15	18	←→	SD15
Ground	19	——	Ground
Keypin	20		No Connection

Table 6-1. AT-Bus Interface Signals (continued)

Drive Connector		Direction	AT System BUS
Signal Name	Pin No.		
DMARQ	21	⟶	DMARQ
Ground	22	——	Ground
IOW-	23	⟵	IOW-
Ground	23	——	Ground
IOR-	25	⟵	IOR-
Ground	26	——	Ground
IORDY	27	⟶	IORDY
Reserved	28		No Connection
DMACK-	29	⟵	DMACK-
Ground	30	——	Ground
INTRQ	31	⟶	INTRQ
IOCS16-	32	⟶	IOCS16-
ADDR1	33	⟵	SA1
PDIAG-	34	*——*	PDIAG-
ADDR0	35	⟵	SA0
ADDR2	36	⟵	SA2
CS1FX-	37	⟵	CS0-
CS3FX-	38	⟵	CS1-
DASP-	39	*⟶	DASP-
Ground	40	——	Ground

* Drive Intercommunication Signals

Drive 1		Drive 0			Host
34	— PDIAG →	34	34	——	34
39	— DASP- →	39	39	⟶	39

Table 6-2 lists the signal name mnemonic, connector pin number, whether input to (I) or output from (O) the drive, and the full signal name.

Table 6-2. Interface Signals Description

Signal	Pin	DIR	Description
CS1FX-	37	I	Drive chip Select 0
CS3FX-	38	I	Drive chip Select 1
DA0	35	I	Drive Address Bus - Bit 0
DA1	33	I	- Bit 1
DA2	36	I	- Bit 2
DASP-	39	I/O	Drive Active/Slave Present
DD0	17	I/O	Drive Data Bus - Bit 0
DD1	15	I/O	- Bit 1
DD2	13	I/O	- Bit 2
DD3	11	I/O	- Bit 3
DD4	9	I/O	- Bit 4
DD5	7	I/O	- Bit 5
DD6	5	I/O	- Bit 6
DD7	3	I/O	- Bit 7
DD8	4	I/O	- Bit 8
DD9	6	I/O	- Bit 9
DD10	8	I/O	- Bit 10
DD11	10	I/O	- Bit 11
DD12	12	I/O	- Bit 12
DD13	14	I/O	- Bit 13
DD14	16	I/O	- Bit 14
DD15	18	I/O	- Bit 15
DIOR-	25	I	Drive I/O Read
DIOW-	23	I	Drive I/O Write

Table 6-2. Interface Signals Description(continued)

Signal	Pin	DIR	Description
DMACK-	29	I	DMA Acknowledge
DMARQ	21	O	DMA Request
INTRQ	31	O	Drive Interrupt
IOCS16-	32	O	Drive 16-bit I/O
IORDY	27	O	I/O Channel Ready
PDIAG-	34	I/O	Passed Diagnostics
RESET-	1	I	Drive Reset
Keypin	20	—	Pin used for keying the interface connector

NOTE : A minus sign follows the name of any signal that is asserted as active low. Direction (DIR) is in reference to the drive:

IN indicates input to the drive.
OUT indicates output from the drive.
I/O indicates that the signal is bi-directional.

6-3 *Logical Interface*

6-3-1 General

6-3-1-1 Bit Conventions

Bit names are shown in all upper case letters except where a lower case n precedes a bit name. This indicates that when nBIT=0 (bit is zero) the action is true and when nBIT=1 (bit is one) the action is false. If there is no preceding n, then when BIT=1 it is true, and when BIT=0 it is false.

A bit can be set to one or cleared to zero and polarity influences whether it is to be interpreted as true or false:

True BIT=1 nBIT=0
False BIT=0 nBIT=1

6-3-1-2 Environment

Data is transferred in parallel (16bits) either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisy chained on the interface, commands are written in parallel to both devices; this is true for all except the Execute Diagnostics command, only the selected device executes the command. On an Execute Diagnostics command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Drives are selected by the DEV bit in the Drive/Head Register (see 6.3.4.9), and by a jumper or switch on the device designating it as either a Device 0 or as Device 1. When DEV=0, Device 0 is selected. When DEV=1, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1. When a single device is attached to the interface it shall be set as Device 0.

Throughout this document, device selection always refers to the state of the DEV bit, the position of the Device 0/Device 1 jumper or switch, or use of the CSEL pin.

A device can operate in either of two addressing modes, CHS or LBA, on a command by command basis. A device which can support LBA mode indicates this in the register, Sector Number register, Cylinder Low mode in the Device/Head register, Sector Number register, Cylinder Low register, Cylinder High register and HS3-HS0 of the Device/Head register contains the zero based-LBA.

This term defines the addressing mode of the device as being by physical sector address.

The physical sector address is made up of three fields: the sector number, the head number and the cylinder number. Sectors are numbered from 0 to a device specific maximum value which cannot exceed 255. Heads are numbered from 0 to a device specific maximum value which cannot exceed 15. Cylinders are numbered from 0 to a device specific maximum value which cannot exceed 65,535. Typically, sequential access to the media is accomplished by treating the sector number as the least significant portion, the head number as the mid-portion, and the cylinder number as the most significant portion of the CHS address.

In LBA (Logical Block Address) mode the sectors on the device are assumed to be linearly mapped with an Initial definition of : LBA 0 = (Cylinder 0, head 0, sector 0). Irrespective of translate mode geometry set by the host, the LBA address of a given sector does not change:

LBA = ((cylinder * heads_per_cylinder + heads) * sectors_per_track) + sector - 1

6-3-2 I/O Register-Address

Communication to or from the drive is through an I/O Register that routes the input or output data to or from registers addressed by a code on signals from the host (CS1FX-, CS3FX-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the drive or posting status from the drive.

The Control Block Registers are used for drive control and to post alternate status. Table 6-3 lists these registers and the addresses that select them.

Table 6-3. I/O Port Function/Selection Address

Address					Functions	
CS1FX-	**CS3FX-**	**DA2**	**DA1**	**DA0**	**READ(DIOR-)**	**WRITE(DIOW-)**
Control Block Registers						
N	N	X	X	X	High Impedance	Not Used
N	A	0	X	X	High Impedance	Not Used
N	A	1	0	X	High Impedance	Not Used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not Used
Command Block Registers						
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features

Table 6-3. I/O Port Function/Selection Address (continued)

Address					Functions	
CS1FX-	CS3FX-	DA2	DA1	DA0	READ(DIOR-)	WRITE(DIOW-)
Command Block Registers						
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	* LBA bits 0-7	* LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	* LBA bits 8-15	* LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	* LBA bits 16-23	* LBA bits 16-23
A	N	1	1	0	Drive/Head	Drive/Head
A	N	1	1	0	* LBA bits 24-27	* LBA bits 24-27
A	N	1	1	1	Status	Command
N	N	X	X	X	Invalid Address	Invalid Address

* Mapping of registers in LBA mode

Logic conventions are :

A = signal asserted
N = signal negated
X = don't care

6-3-3 Control Block Register Descriptions

6-3-3-1 Alternate Status Register (3F6h)

This register contains the same information as the Status Register in the command block. The only difference being that reading this register does not imply interrupt acknowledgment nor clear a pending interrupt.

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	BSY	DRQ	CORR	IDX	ERR

NOTE : See section 6.3.4.10 for definitions of the bits in this register.

6-3-3-2 Drive Address Register (3F7h)

This register contains the inverted drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

7	6	5	4	3	2	1	0
HiZ	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

- **HiZ** is always in a high impedance state.
- **nWTG** is the Write Gate bit. When writing to the disk drive is in progress, nWTG=0.
- **nHS3 through nHS0** are the one's complement of the binary coded address of the currently selected head. For example, if nHS3 through nHS0 are 1100b, respectively, head 3 is selected. nHS3 is the most significant bit.
- **nDS1** is the drive select bit for drive 1. When drive 1 is selected and active, nDS1=0.
- **nDS0** is the drive select bit for drive 0. When drive 0 is selected and active, nDS0=0.

NOTE : Caching, translation and master / slave may cause this register to contain invalid data.

6-3-3-3 Device Control Register (3F6h)

The bits in this register are as follows:

7	6	5	4	3	2	1	0
X	X	X	X	1	SRST	nIEN	0

- **SRST** is the host software reset bit. The drive is held reset when this bit is set. If two disk drives are daisy chained on the interface, this bit resets both simultaneously.
- **nIEN** is the enable bit for the drive interrupt to the host. When nIEN=0, and the drive is selected, INTRQ is enabled through a tri-state buffer. When nIEN=1, or the drive is not selected, the INTRQ signal is in a high impedance state.

6-3-4 Command Block Register Descriptions

6-3-4-1 Data Register (1F0h)

This 16-bit register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command. Data transfers may be either PIO or DMA.

6-3-4-2 Features Register (1F1h)

This register is command specific and used to enable and disable features of the interface (e.g. by the Set Features command to enable and disable caching).

6-3-4-3 Sector Number Register (1F3h)

In **CHS** mode this register contains the starting sector number for any disk data access for the subsequent command. The sector number is from 1 to the maximum number of sectors per track. In **LBA** mode this register contains bits 0-7 of the LBA.

See the command descriptions for contents of the register at command completion (whether successful or unsuccessful).

6-3-4-4 Error Register (1F1h)

This register contains status from the last command executed by the drive or a Diagnostic Code.

At the completion of any command except Execute Drive Diagnostic, the contents of this register are valid when ERR=1 in the Status Register.

Following a power on, a reset, or completion of an Execute Drive Diagnostic command, this register contains a Diagnostic Code (see Table 6-5).

7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

- **BBK (Bad Block Detected)** indicates a bad block mark was detected in the requested sector's ID field.
- **UNC (Uncorrectable Data Error)** indicates an uncorrectable data error has been encountered.
- **IDNF (ID Not Found)** indicates the requested sector's ID field could not be found.
- **ABRT (Aborted Command)** indicates the requested command has been aborted due to a drive status error (Not Ready, Write Fault, etc.) or because the command code is invalid.
- **K0NF (Track 0 Not Found)** indicates track 0 has not been found during a Recalibrate command.
- **AMNF (Address Mark Not Found)** indicates the data address mark has not been found after finding the correct ID field.

NOTE : Unused bits are cleared to zero.

6-3-4-5 Sector Count Register (1F2h)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the drive. If the value in this register is zero, a count of 256 sectors is specified.

If this register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of this register may be defined otherwise on some commands (e.g. Initialize Drive Parameters, Format Track commands).

6-3-4-6 Cylinder High Register (1F5h)

In **CHS** mode this register contains the high order bits of the starting cylinder address for any disk access. In **LBA** mode this register contains bits 8-15 of the LBA.

At the end of the command, this register is updated to reflect the current disk address. The most significant bits of the cylinder address are loaded into the Cylinder High Register.

6-3-4-7 Cylinder Low Register (1F4h)

In **CHS** mode this register contains the low order 8 bits of the starting cylinder address for any disk access. In **LBA** mode this register contains bits 16-23 of the LBA. At the end of the command, this register is updated to reflect the current disk address.

6-3-4-8 Command Register (1F7h)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 6-4.

6-3-4-9 Drive/Head Register (1F6h)

This register contains the drive and head numbers. When executing an Initialize Drive Parameters command, the contents of this register defines the number of heads minus 1.

7	6	5	4	3	2	1	0
1	LBA	1	DEV	HS3	HS2	HS1	HS0

- **DRV** is the binary encoded drive select number. When DEV=0, Device 0 is selected. When DEV=1, Device 1 is selected.

- **HS3 through HS0** contain the binary coded address of the head to be selected in **CHS** mode (e.g. if HS3 through HS0 are 0011b, respectively, head 3 will be selected. HS3 is the most significant bit). In **LBA** mode this register contains bits 24-27 of the LBA. At command completion, this register is updated to reflect the currently selected disk address.

- **LBA** is the binary coded address mode select. When L=0, disk addressing is by **CHS** mode. When L=1, disk addressing is by **LBA** mode. This bit was set to zero when ATA drive didn't supported LBA mode

6-3-4-10 Status Register (1F7h)

This register contains the drive status. The contents of this register are updated at the completion of each command. When BSY is cleared, the other bits in this register are valid within 400 nsec. If BSY=1, no other bits in this register are valid. If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

NOTE : If Drive 1 is not detected as being present, Drive 0 clears the Drive 1 Status Register to 00h (indicating that the drive is Not Ready).

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

- **BSY (Busy)** is set whenever the drive has access to the Command Block Registers. The host should not access the Command Block Register when BSY=1. When BSY=1, a read of any Command Block Register returns the contents of the Status Register. This bit is set by the drive under the following circumstances:

a) within 400 nsec after the negation of RESET- or after SRST has been set in the Device Control Register.

b) within 400 nsec of a host write of the Command Register with a Read, Read Long, Read Buffer, Seek, Recalibrate, Initialize Drive Parameters, Read Verify, Identify Drive, or Execute Drive Diagnostic command.

c) within 5 μsec following transfer of 512 bytes of data during execution of a Write, Format Track, or Write Buffer command, or 512 bytes of data and the appropriate number of ECC bytes during the execution of a Write Long command.

- **DRDY (Drive Ready)** indicates that the drive is capable of responding to a command. When there is an error, this bit does not change until the host reads the Status Register. Then the bit again indicates the current readiness of the drive. This bit clear at power on and remains clear until the drive is ready to accept a command.

- **DWF (Drive Write Fault)** indicates the current write fault status. When an error occurs, this bit is not changed until the Status Register is read by the host, at which

time the bit again indicates the current write fault status.

- **DSC (Drive Seek Complete)** indicates that the drive heads have settled over a track. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current Seek Complete status.

- **DRQ (Data Request)** indicates that the drive is ready to transfer a word or byte of data between the host and the drive.

- **CORR (Corrected Data)** indicates that a correctable data error was encountered and the data has been corrected. This condition does not terminate a data transfer.

- **IDX (Index)** is set once per disk revolution.

- **ERR (Error)** indicates that an error occurred during execution of the previous command. The bits in the Error Register have additional information regarding the cause of the error.

6-4 *At Command Register Descriptions*

Commands are issued to the drive by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 6-4) of command acceptance, all based on the fact that to receive a command, BSY=0:

- Upon receipt of a Class 1 command, the drive sets BSY within 400 nsec
- Upon receipt of a Class 2 command, the drive sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears BSY within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the drive sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec, and clears BSY within 400 nsec of setting DRQ.

NOTE : DRQ may be set so quickly on Class 2 and Class 3 that the BSY transition is too short for BSY=1 to be recognized.

If a new command is issued to a drive which has an uncompleted command (subsequently referred to as Old_Command) in progress, the drive immediately responds to the new command (Subsequently referred to as New_Command), even if execution of the Old_Command could have been completed.

Table 6-4. Command Codes and Parameters

	COMMAND		PARAMETER USED				
Class	DESCRIPTION	CODE	FR	SC	SN	CY	DH
1	Execute Device Diagnostic	90h					D*
2	Format Track	50h					d
1	Identify Device	ECh					D
1	Idle	97h,E3h		y			D
1	Idle Immediate	95h,E1h					D
1	Initialize Drive Parameter	91h		y			y
1	Read Buffer	E4h					
1	Read DMA (w/retry)	C8h		y	y	y	y
1	Read DMA (w/o retry)	C9h		y	y	y	y

Table 6-4. Command Codes and Parameters (continued)

	COMMAND		PARAMETER USED				
Class	DESCRIPTION	CODE	FR	SC	SN	CY	DH
1	Recalibrate	1xh					D
1	Read Multiple	C4h		y	y	y	y
1	Read Sector(s) (w / retry)	20h		y	y	y	y
1	Read Sector(s) (w / o retry)	21h		y	y	y	y
1	Read Long (w / retry)	22h		y	y	y	y
1	Read Long (w / o retry)	23h		y	y	y	y
1	Read Verify Sector(s) (w / retry)	40h		y	y	y	y
1	Read Verify Sector(s) (w / o retry)	41h		y	y	y	y
1	Seek	7xh			y	y	y
1	Set Features	EFh	y				D
1	Set Multiple Mode	C6h		y			D
1	Sleep Mode	99h,E6h					D
1	Standby	96h,E2h		y			D
1	Standby Immediate	94h,E0h					D
2	Write Buffer	E8h					D
3	Write DMA (w / retry)	CAh		y	y	y	y
3	Write DMA (w / o retry)	CBh		y	y	y	y
3	Write Multiple	C5h	*	y	y	y	y
2	Write Sector(s) (w / retry)	30h	*	y	y	y	y
2	Write Sector(s) (w / o retry)	31h	*	y	y	y	y
2	Write Long (w / retry)	32h	*	y	y	y	y
2	Write Long (w / o retry)	33h	*	y	y	y	y
3	SMART Commands	0B0h	*				

CY = Cylinder Register SC = Sector Count Register
DH = Device / Head Register SN = Sector Number Register
FR = Feature Register
y - The register contains a valid parameter for this command. For the Device / Head Register, y means both the device and head parameters are used.
D - Only the drive parameter is valid and not the head parameter,

d - The device parameter is valid, the usage of the head parameter is vendor specific.
D* - Address to Device 0 but both devices execute it.
* - Maintained for compatibility

6-4-1 Check Power Mode (98h,E5h)

This command checks the power mode.

If the drive is in, going to, or recovering from the Standby Mode the drive sets BSY, sets the Sector Count Register to 00h, clears BSY, and generates an interrupt.

If the drive is in the Idle Mode, the drive sets BSY, sets the Sector Count Register to FFh, clears BSY, and generates an interrupt.

6-4-2 Execute Device Diagnostics (90h)

This command performs the internal diagnostic tests implemented by the drive. The DRV bit is ignored. Both drives, if present, shall execute this command.

If Drive 1 is present:

- Drive 1 asserts PDIAG- within 5 seconds.
- Drive 0 waits up to 6 seconds for Drive 1 to assert PDIAG-.
- If Drive 1 has not asserted PDIAG-, indicating a failure, Drive 0 appends 80h to its own diagnostic status.
- Both drives execute diagnostics.
- If Drive 1 diagnostic failure is detected when Drive 0 status is read, Drive 1 status is obtained by setting the DRV bit, and reading status.

If there is no Drive 1 present:

- Drive 0 posts only its own diagnostic results.
- Drive 0 clears BSY, and generates an interrupt.

The Diagnostic Code written to the Error Register is a unique 8-bit code (shown in Table 6-5) not as the single bit flags defined in 6.3.4.4.

If Drive 1 fails diagnostics, Drive 0 "ORs" 80h with its own status and loads that code into the Error Register. If Drive 1 passes diagnostics or there is no Drive 1 connected, Drive 0 "ORs" 00h with its own status and loads that code into the Error Register.

Table 6-5. Diagnostic Codes

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controlling microprocessor error
8xh	Drive 1 failed

6-4-3 Format Track (50h)

The track address is specified in the Cylinder High and Cylinder Low Registers, and the number of sectors is specified in the Sector Count Register. When the command is accepted, the drive sets the DRQ bit and waits for the host to fill the sector buffer. When the sector buffer is full, the drive clears DRQ, sets BSY and begins command execution. WN310820A / WN321620A hard disk drives write zeros to the data fields in the sectors on the specified logical track. The ID fields are not written by this command.

6-4-4 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the device. When the command is issued, the device sets BSY bit, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host cab then transfer the data by reading the Data register. The parameter words in the buffer have the arrangement and meanings defined in Table 6-6. All reserved bits or words shall be zero.

The F / V column indicates if the word or part of a word had fixed (F) contents that do not change, variable (V) contents that may change depending on the device state or the commands executed by the device, X for words with vendor specific data which may be fixed or variable, and R for reserved words which shall be zero. For removable media devices, the value of fields indicated as fixed (F) may change when media is removed or changed.

Some parameters are defined as a group of bits. A word which is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a sixteen bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bits DD15 and the least significant bit on bit DD0.

Some parameters are defines as 32 bit value (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD15 through DD0 respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD15 through DD0 respectively.

Some parameters are defined as a string of ASCII characters. For the string "Copyright", the character 'C' is the first byte, '0' is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character ('C') is on bits DD15 through DD8 of the first word
the 2nd character ('o') is on bits DD7 through DD0 of the first word
the 3rd character ('p') is on bits DD15 through DD8 of the second word
the 4th character ('y') is on bits DD7 through DD0 of the second word
etc.

6-4-4-1 Word 1 : Number of cylinders

The number of user-addressable logical cylinders in the default translation mode.

6-4-4-2 Word 3 : Number of logical heads

The number of user-addressable logical heads in the default translation mode.

6-4-4-3 Word 6 : Number of logical sectors per logical track

The number of user-addressable sectors per logical track in the default translation mode.

6-4-4-4 Word 10-19 : Serial Number

If word 10 of this field is 0000h, then the serial number is not specified and the definition of the remaining words of this field are vendor specific.

If word 10 of this field is net equal to 0000h, then this field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

6-4-4-5 Word 22 : Number of vendor specific bytes on Read/Write Long commands

The contents of this field specifies the number of vendor specific bytes that are appropriate for the device. If the contents of this field are set to a value other than 4, the SET FEATURES command should be used to switch the length of READ LONG and WRITE LONG commands from 512 plus 4 to 512 plus the value specified in this word.

6-4-4-6 Word 23-26 : Firmware revision

If word 23 of this field is 0000h, then the firmware revision is not specified and the definition of the remaining words of this field are vendor specific.

If word 23 of this field is not equal to 0000h, then this field contains the firmware revision of the device. The contents of this field is an ASCII character string of eight bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

6-4-4-7 Word 27-46 : Model Number

If word 27 of this field is 0000h, then the model number is not specified and the definition of the remaining words of this field are vendor specific.

If word 27 this field is not equal to 0000h, then this field contains the model number of the device. The contents of this field is an ASCII character string of forty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

6-4-4-8 Word 47 : Read/Write Multiple support

Bits 7-0 of this word define the maximum number of sectors per block that the device supports for READ / WRITE MULTIPLE commands. If a device supports the READ / WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits contain a non-zero value. If the device does not support the READ / WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits shall be zero.

6-4-4-9 Word 49 : Capabilities

6-4-4-9-1 Standby Timer Support

Bit 13 of word 49 is used to determine whether a device utilizes the Standby Timer values defined in this standard. If bit 13 is set to one, then the device utilizes the Standby Timer values as specified in Table 13 (see clause 8.11). If bit 13 is set to zero, the timer values utilized are vendor specific.

6-4-4-9-2 IORDY Support

Bit 11 of word 49 is used to help determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This insures backward compatibility. This device supports PIO Mode 3, so this bit shall be set.

6-4-4-9-3 IORDY Can Be Disabled

Bit 10 of word 49 is used to indicate a device's ability to enable disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Control of IORDY is accomplished using the SET FEATURES command.

6-4-4-9-4 LBA Supported

Bit 9 of word 49 is used to indicate if the device supports LBA mode addressing. If this bit is set, words 60-61 shall be valid.

6-4-4-9-5 DMA Supported

Bit 8 of word 49 is used to indicate of the device supports the READ / WRITE DMA commands.

6-4-4-10 Word 51 : PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 10 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 4 categories specified in figure 10, and if it does not, then Mode 0 shall be used to serve as the default timing. Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, 2, 3 or 4) it can support.

6-4-4-11 Word 52 : Single Word DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 11 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 11 (i.e. 0, 1 or 2), and if it does not, then Mode 0 shall be used to serve as the default timing.

6-4-4-12 Word 53 : Field Validity

If bit 0 of word 53 is set, then the values reported in words 54 through 58 are valid. If this bit is cleared, the values reported in words 54 through 58 may be valid. If bit 1 of word 53 is set, then the values reported in words 64 through 70 are valid. If this bit is cleared, the values reported in words 64-70 are not valid. Any device which supports PIO modes 3 or above, or supports Multi-word DMA Mode 1 or above, shall set bit 1 of word 53 and support the fields contained in words 64 through 70.

6-4-4-13 Word 54 : Number of current logical cylinders

The number of user-addressable logical cylinders in the current translation mode.

6-4-4-14 Word 53 : Number of current logical heads

The number of user-addressable logical heads per logical cylinder in the current translation mode.

6-4-4-15 Word 56 : Number of current logical sectors per logical track

The number of user-addressable logical sectors per logical track in the current translation mode.

6-4-4-16 Word 57-58 : Current capacity in sector

The current capacity in sectors excludes all sectors used for device-specific purposes. The value reported in this field shall be the product of words 54, 55 and 56.

6-4-4-17 Word 59 : Multiple sector setting

If the valid bit is set, then bits 7-0 reflect the number of sectors currently set to transfer on a Read / Write Multiple command. If word 47 bits 7-0 are zero then word 59 bits 8-0 shall also be zero.

6-4-4-18 Word 60-61 : Total number of user addressable sectors

If the device supports LBA Mode, these words reflect the total number of user addressable sectors. This value does not depend on the current device geometry. If the device does not support LBA mode, these words shall be set to 0.

6-4-4-19 Word 62 : Single word DMA transfer

The low order byte identifies by bit all of the Modes which are supported (e.g. if Mode 0 is supported, bit 0 is set). The high order byte contains a single bit set to indicate which mode is active.

6-4-4-20 Word 63 : Multiword DMA transfer

The low order byte identifies by bit all the supported Modes, for example if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

6-4-4-21 Word 64 : Flow Control PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Device Parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes that it is capable of supporting.

6-4-4-22 Word 65 : Minimum Multiword DMA Transfer Cycle Time Per Word

Word 65 of the parameter information of the IDENTIFY DEVICE Command is defined as the minimum Multi-word DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multi-word DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multi-word DMA Mode 1 or above shall support this field, and the value in word 65 shall not

be less than the minimum cycle time reported by the fastest DMA mode supported by the device.

6-4-4-23 Word 66: Manufacture's Recommended Multi-word DMA Cycle Time

Word 66 of the parameter information of the IDENTIFY DEVICE Command is defined as the Manufacture's Recommended Multi-word DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under nominal conditions.

If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does ensure that flow control will not be used, but implies that higher performance MAY result.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multi-word DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

6-4-4-24 Word 67 : Minimum PIO Transfer Cycle Time Without Flow Control

Word 67 of the parameter information of the IDENTIFY DEVICE Command is defined as the Minimum PIO Transfer without Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

6-4-4-25 Word 68 : Minimum PIO Transfer Cycle Time With IORDY

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer with IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

Any device may support this field, and if this is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above must this field, and the value in word 68 shall not be less than the fastest PIO mode reported bythe device.

Table 6-6. Identify Device Information

Word	Description
0	General configuration bit-significant information: 15 0 reserved for non-magnetic devices 14 vendor specific (obsolete) 13 vendor specific (obsolete) 12 vendor specific (obsolete) 11 vendor specific (obsolete) 10 vendor specific (obsolete) 9 vendor specific (obsolete) 8 vendor specific (obsolete) 7 1=removable media device 6 1=not removable controller and/or device 5 vendor specific (obsolete) 4 vendor specific (obsolete) 3 vendor specific (obsolete) 2 vendor specific (obsolete) 1 vendor specific (obsolete) 0 Reserved
1	Number of logical cylinders
2	Reserved
3	Number of logical heads
4	Vendor specific (obsolete)
5	Vendor specific (obsolete)
6	Number of logical sectors per logical track
7-9	Vendor specific
10-19	Serial number
20	Vendor specific (obsolete)
21	Vendor specific (obsolete)
22	# of vendor specific bytes avail on READ/WRITE LONG cmds

Table 6-6. Identify Drive Information (continued)

Word	Description
23-26	Firmware revision (8 ASCII characters)
27-46	Model number (40 ASCII characters)
47	15-8 vendor specific 7-0 00h = READ / WRITE MULTIPLE commands not implemented 01h-FEh = Maximum number of sectors that can be transferred per interrupt per interrupt on READ MULTIPLE and WRITE MULTIPLE commands
48	Reserved
49	Capabilities 15-14 Reserved 13 1=Standby time values as specified in this standard are supported 0=Standby timer values are vendor specific 12 Reserved (for advanced PIO mode support) 11 1=IORDY supported 0=IORDY may be supported 10 1=IORDY can be disabled 9 1=LBA supported 8 1=DMA supported 7-0 Vendor specific
50	Reserved
51	15-8 PIO data transfer cycle timing mode 7-0 Vendor specific
52	15-8 DMA data transfer cycle timing mode 7-0 Vendor specific
53	15-2 Reserved 1 1 = the fields reported in words 64-70 are valid 0 = the fields reported in words 64-70 are not valid 0 1 = the fields reported in words 54-58 are valid 0 = the fields reported in words 54-58 may be valid
54	Number of current logical cylinders

Table 6-6. Identify Drive Information (continued)

Word	Description
55	Number of current logical heads
56	Number of current sectors per track
57-58	Current capacity in sectors
59	15-9 Reserved
	8 1 = Multiple sector setting is valid
	7-0 xxh = Current setting for number of sectors that can be transferred per interrupt on R/W multiple commands
60-61	Total number of user addressable sectors (LBA mode only)
62	15-8 Single word DMA transfer mode active
	7-0 Single word DMA transfer modes supported
63	15-8 Multiword DMA transfer mode active
	7-0 Multiword DMA transfer modes supported
64	15-8 Reserved
	7-0 Advanced PIO transfer modes supported
65	Minimum Multiword DMA xfer cycle time per Word
	15-0 Cycle time in nanoseconds
66	Mfg.'s recommended Multiword DMA xfer cycle time
	15-0 Cycle time in nanoseconds
67	Minimum PIO xfer cycle time without flow control
	15-0 Cycle time in nanoseconds
68	Minimum PIO xfer cycle time with IORDY flow control
	15-0 Cycle time in nanoseconds
69-70	Reserved (for advanced PIO mode support)
71-127	Reserved
128-159	Vendor specific
160-255	Reserved

6-4-5 Idle (97h,E3h)

This command causes the drive to set BSY, enter the Idle Mode, clear BSY, and generate an interrupt. The interrupt is generated even though the drive may not have fully transitioned to Idle Mode.

If the drive is already spinning, the spin-up sequence is not executed.

If the Sector Count Register is non-zero, the automatic Idle Mode sequence is enabled and the timer begins counting down immediately. If the Sector Count Register is zero, the automatic power down sequence is disabled.

After the drive entered the Idle Mode, it automatically transitions to the Standby Mode upon expiration of a prescribed 1 minute spin-down timer.

Table 6-7. Automatic Standby Timer Periods

Sector Count Register Contents	Corresponding Time-out Period
0 (00h)	Timeout Disabled
1-240 (01h-FOh)	(value * 5) seconds
241-251 (F1h-FBh)	((value - 240) * 30) minutes
252 (FCh)	21 minutes
253 (FDh)	8 hours
254 (FEh)	Reserved
255 (FFh)	21 minutes 15 seconds

6-4-6 Idle Immediate (95h,E1h)

This command causes the drive to set BSY, enter the Idle Mode, clear BSY, and generate an interrupt. The interrupt is generated even though the drive may not have fully transitioned to Idle Mode.

6-4-7 Initialize Device Parameters (91h)

This command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Upon receipt of the command, the drive sets BSY, saves the parameters, clears BSY, and generates an interrupt.

The only two register values used by this command are the Sector Count Register which specifies the number of sectors per track, and the Drive / Head Register which specifies the number of heads minus 1. The DRV bit designates these values to Drive 0 or Drive 1, as appropriate.

The sector count and head values are not checked for validity by this command. If they are invalid, no error will be posted until an illegal access is made by some other command.

6-4-9 Recalibrate (1xh)

This command moves the read / write heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive sets BSY and issues a seek to cylinder zero. The drive then waits for the seek to complete before updating status, clearing BSY and generating an interrupt. If the drive cannot reach cylinder 0, it posted a Track 0 Not Found error.

6-4-10 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the drive's sector buffer. When this command is issued, the drive sets BSY, sets up the sector buffer for a read operation, sets DRQ, clears BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.
The Read Buffer and Write Buffer commands are be synchronized so that sequential Write Buffer (E8h) and Read Buffer commands access the same 512 bytes within the buffer.

6-4-11 Read DMA (C8h)

This command executes in a similar manner to the Read Sector(s) command except for the following:

- the host initializes a slave-DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- the drive issues only one interrupt per command to indicate that data transfer has stopped and the status is available.

Any unrecoverable error encountered during execution of a Read DMA command results in the termination of data transfer prior to at the sector where the error was detected. The drive generates an interrupt to indicate that data transfer has terminated and status is available. The error posting is the same as that of the Read Sector(s) command.

6-4-12 Read Long (22h)

The Read Long command performs similarly to the Read Sectors command except that it returns the data and the ECC bytes appended to the data field of the desired sector. During a Read Long command, the drive does not check the ECC bytes to determine if there has been a data error. Only single sector Read Long operations are supported.

The transfer of the ECC bytes shall be 8 bits wide, and 4 or 11 bytes long.

6-4-13 Read Multiple Command (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which should be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where

n = Remainder (Sector Count / Block Count)

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error.

Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer takes place as it normally would, including transfer of corrupted data, if any.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

6-4-14 Read Sector(s) (20h)

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. See 6.6.1 for the DRQ, IRQ and BSY protocol on data transfers.

If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field.

If retries are disabled and two index pulses have occurred without error free reading of the requested ID, an ID Not Found error is posted.

If retries are enabled, up to a vender specified number of attempts are made to read the requested ID before posting an error.

If the ID is read correctly, the data address mark shall be recognized within a specified number of bytes, or the Address Mark Not Found error is posted. DRQ is always set prior to data transfer regardless of the presence or absence of an error condition.

At command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector read in CHS mode, or logical block address in LBA mode.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred in CHS mode, or logical block address in LBA mode. The flawed data is pending in the sector buffer.

6-4-15 Read Verify Sector(s) (40h)

This command is identical to the Read Sectors command, except that DRQ is never set, and no data is transferred to the host. See 6.6.3 for protocol. When the command is accepted, the drive sets BSY.

When the requested sectors have been verified, the drive clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified in CHS mode, logical block address in LBA mode. If an error occurs, the verify terminates at the sector where the error occurs.

The Command Block Registers contain the cylinder, head, and sector number in CHS mode, or logical block address in LBA mode where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6-4-16 Seek (7xh)

This command initiates a seek to the track and selects the head specified in the command block. The drive need not be formatted for a seek to execute properly. Refer to section 6.6.3 for protocol. The drive shall not set DSC=1 until the action of seeking has completed. The drive may return the interrupt before the seek is completed.

If another command is issued to the drive while a seek is being executed, the drive sets BSY=1, waits for the seek to complete, and then begins execution of the command.

6-4-17 Set Features (EFh)

This command is used by the host to establish the following parameters which affect the execution of certain drive features as shown in Table 6-8.

Table 6-8. Set Feature Register Definitions

Code	Description
02h	Enable Write Cache
03h	Set transfer mode based on value in Sector Count register
33h	Disable Retry
44h	11 bytes of ECC apply on Read Long / Write Long commands
55h	Disable read look-ahead feature
77h	Disable ECC
82h	Disable Write Cache
88h	Enable ECC
99h	Enable Retries
AAh	Enable read look-ahead feature
BBh	4 bytes of ECC apply on Read Long / Write Long commands

When the drive receives this command, it sets BSY, checks the contents of the Feature register, clears BSY, and generates an interrupt. If the value in the Feature Register is not supported or is invalid, the drive posts an Aborted Command error. Refer to section 6.6.3 for protocol.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count Register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

Block transfer (default)	00000	000
Single word DMA Mode x	00010	0xx
Multi-word DMA Mode 0	00100	000

6-4-18 Set Multiple Mode (C6h)

This command enables the drive to perform Read and Write Multiple operations and establishes the block count for these commands. Refer to section 6.6.3 for protocol.

The Sector Count Register is loaded with the number of sectors per block. Drives

support block sizes of 2, 4, 8, and 16 sectors. Upon receipt of the command, the drive sets BSY=1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled.

If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware reset, the default mode is Read and Write Multiple disabled. And on software reset, the default mode of Read and Write Multiple will not be changed.

6-4-19 Sleep (99h,E6h)

This command is the only way to cause the drive to enter Sleep Mode. The drive is spun down, and when it is stopped, BSY is cleared, an interrupt is generated, and the interface becomes inactive.

The only way to recover from Sleep mode without a reset or power on, is for the host to issue a software reset.

A drive shall not power on in Sleep Mode nor remain in Sleep Mode following a reset sequence. If the drive is already spun down, the spin down sequence is not executed.

6-4-20 Standby (96h,E2h)

This command causes the drive to set BSY, enter the Standby Mode, clear BSY, and asserted INTRQ. INTRQ is isserted even though the device may not have fully transitioned to Standby Mode.

If the Sector Count Register is non-zero, then the Standby Timer shall enabled. The value in the Sector Count register shall be used to determine time programmed into the Standby Mode.

The value in the Sector Count Register when the STANDBY command is issued shall determine the time period programmed into the Standby Timer. See Table 6-7.

6-4-21 Standby Immediate (94h,E0h)

This command causes the drive to enter the Standby Mode. See 6.6.3 for protocol. The drive may return the interrupt before the transition to Standby Mode is completed.

If the drive is already spun down, the spin down sequence is not executed.

6-4-22 Write Buffer (E8h)

This command enables the host to overwrite the contents of the drive's sector buffer with any data pattern desired. See 6.6.2 for protocol.

The Read Buffer and Write Buffer commands shall be synchronized within the drive such that sequential Write Buffer and Read Buffer commands access the same 512 bytes within the buffer.

6-4-23 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The drive sets BSY within 400 nsec of accepting the command, and interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple.

Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = Remainder (Sector Count / Block Count)

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation is rejected with an aborted command error.

Disk errors encountered during execution of Write Multiple commands are posted after the attempted disk write of the block or partial block transferred. The Write Multiple command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

6-4-24 Write DMA (CAh)

This command executes in a similar manner to Write Sector(s) except for the following

- the host initializes a slave-DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- the drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

Any error encountered during Write DMA execution results in the termination of data transfer. The drive issues an interrupt to indicate that data transfer has terminated and status is available in the Error Register. The error posting is the same as that of the Write Sector(s) command.

6-4-25 Write Long (32h)

This command is similar to the Write Sectors command except that it writes the data and the ECC bytes directly from the sector buffer; the drive does not generate the ECC bytes itself. Only single sector Write Long operations are supported.

The transfer of the ECC bytes shall be 8 bits wide, and 4 or 11 bytes long.

6-4-26 Write Sector(s) (30h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register (a sector count of zero requests 256 sectors), beginning at the specified sector. Refer to Section 6.7 for the DRQ, IRQ and BSY protocol on data transfers.

If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field.

If retries are disabled and two index pulses have occurred without error free reading of the requested ID, an ID Not Found error is posted.

If retries are enabled, up to a predefined number of attempts may be made to read the requested ID before posting an error.

If the ID is read correctly, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector written in CHS mode, logical block address in LBA mode.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred in CHS mode, logical block address in LBA mode. The host may then read the command block to determine what

error has occurred, and on which sector.

6-5 *Programming Requirements*

6-5-1 Reset Response

A reset is accepted within 400 nsec after the negation of RESET- or within 400 nsec after SRST has been set in the Device Control Register.

When the drive is reset by RESET-, Drive 1 indicates it is present by asserting DASP- within 400 msec, and DASP- remains asserted for 30 seconds or until Drive 1 accepts the first command.

When the drive is reset by SRST, the drive sets BSY=1. See also Device Control Register (6.3.3.3).

When a reset is accepted, and with BSY set:

a) Both drives perform hardware initialization

b) Both drives clear any previously programmed drive parameters

c) Both drives may revert to the default condition

d) Both drives load the Command Block Registers with their default values

e) If a hardware reset, Drive 0 waits for DASP- to be asserted by Drive 1

f) If operational, Drive 1 asserts DASP-

g) Drive 0 waits for PDIAG- to be asserted if Drive 1 asserts DASP-

h) If operational, Drive 1 clears BSY

i) If operational, Drive 1 asserts PDIAG-

j) Drive 0 clears BSY

No interrupt is generated when initialization is complete.

The default values for the Command Block Registers if no self-tests are performed or if no errors occurred are:

Error	=	01h	Cylinder Low	=	00h
Sector Count	=	01h	Cylinder High	=	00h
Sector Number	=	01h	Drive / Head	=	00h

The Error Register contains a Diagnostic Code (see Table 6-5)
Following any reset, the host should issue an Initialize Drive Parameters command to ensure the drive is initialized as desired.

6-5-2 Error Posting

The errors that are valid for each command are defined in Table 6-7.
See 6.3.4.4 and 6.3.4.10 for the definition of the Error Register and Status Register bits.

Table 6-9. Command Errors

Command	Error Register						Status Register				
	BBK	UNC	IDNF	ABRT	TK0NF	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V			V	V	V		V
Execute Drive Diags											V
Format Track			V	V			V	V	V		V
Identify Drive				V			V	V	V		V
Idle				V			V	V	V		V
Idle Immediate				V			V	V	V		V
Initialize Drive Parms							V	V	V		
NOP				V							
Recalibrate				V	V		V	V	V		V
Read Buffer				V			V	V	V		V
Read DMA	V	V	V	V		V	V	V	V	V	V
Read Long	V		V	V		V	V	V	V		V
Read Multiple	V	V	V	V		V	V	V	V	V	V
Read Sector(s)	V	V	V	V		V	V	V	V	V	V
Read Verify Sector(s)	V	V	V	V		V	V	V	V	V	V
Seek			V	V			V	V	V		V
Set Features				V			V	V	V		V
Set Multiple Mode				V			V	V	V		V
Sleep				V			V	V	V		V
Standby				V			V	V	V		V
Standby Immediate				V			V	V	V		V
Write Buffer				V			V	V	V		V
Write DMA	V		V	V			V	V	V		V
Write Long	V		V	V			V	V	V		V
Write Multiple	V		V	V			V	V	V		V

Table 6-9. Command Errors (continued)

Command	Error Register						Status Register				
	BBK	UNC	IDNF	ABRT	TK0NF	AMNF	DRDY	DWF	DSC	CORR	ERR
Write Sector(s)	V		V	V			V	V	V		V
Write Verify	V	V	V	V		V	V	V	V	V	V
Invalid Command Code				V			V	V	V		V

V	=	Valid on this command	AMNF	=	Data address mark not found
BBK	=	Bad block detected	DRDY	=	Drive not ready detected
UNC	=	Uncorrectable data error	DWF	=	Drive write fault detected
IDNF	=	Requested ID not found	DSC	=	Disk seek complete not detected
ABRT	=	Abort command error	CORR	=	Corrected data error
TK0NF	=	Track zero not found error	ERR	=	Error bit in the Status Register

6-5-3 Power Conditions

Winner 3A reduces the power required to operate as shown in Table 6-10, which describes operating mode and the status of major components.

Table 6-10. Power Saving Mode

MODE	R/W	Spindle	VCM	Interface
SLEEP	OFF	OFF	OFF	Disk OFF Host ON
STANDBY	OFF	OFF	OFF	Disk OFF Host ON
IDLE	OFF	ON	OFF	Disk OFF Host ON
NORMAL	ON	ON	ON	ON

6-5-3-1 Sleep mode

When a Sleep command is received, the drive enters the Sleep mode.

The lowest power consumption occurs in Sleep mode. When in Sleep mode, the drive requires a reset to be activated (see 6.4.18).

6-5-3-2 Standby mode

When a Standby command is received, or Auto-Power Down sequence is enabled and Auto-Power Down Count is zero, then the drive enters the Standby mode.

In Stand-By mode, the drive interface is capable of accepting commands, but the media is not immediately accessible.

6-5-3-3 Idle mode

When an Idle command is received, or Auto-Power Down sequence is enabled and Auto-Power Down Count is zero, then the drive enters the Idle mode immediately.

After the drive entered the Idle Mode, it automatically transitions to the Standby Mode upon expiration of a prescribed 1 minute spin-down counter.

In the Idle mode, the drive is capable of responding immediately to media access requests. A drive in Idle mode may take longer to complete the execution of a command than in Normal mode because it may have to activate ENDEC and R/W circuit.

6-5-3-4 Normal mode

In Normal mode, the drive is capable of responding immediately to media access requests, and commands complete execution in the shortest possible time.

See specific power-related commands (6.4).

The power conditions in each mode is as shown in Table 6-11.

Table 6-11. Power Conditions

MODE	SRST	BSY	DRDY	Interface Active	Media
SLEEP	*	x	x	*	0
STANDBY	x	0	1	Yes	0
IDLE	x	0	1	Yes	1
NORMAL	x	x	x	Yes	1

* : See 6.4.18
1 : Active
0 : Inactive
x : don't care

6-6 *Protocol Overview*

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if BSY=1, and should proceed no further unless and until BSY=0. For most commands, the host will also wait for DRDY=1 before proceeding. Those commands shown with DRDY=X can be executed when DRDY=0.

6-6-1 PIO Data in Commands

This class includes:

- Identify Drive (ECh)
- Read Buffer (E4h)
- Read Long (22h)
- Read Sector(s) (20h)
- Read Multiple (C4h)

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the drive to the host.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive / Head registers.

b) The host writes the command code to the Command Register.

c) The drive sets BSY and prepares for data transfer.

d) When a sector of data is available, the drive sets DRQ and cleans BSY prior to asserting INTRQ.

e) After detecting INTRQ, the host reads the Status Register, then reads on sector of data via the Data Register. In response to the Status Register being read, the drive negates INTRQ.

f) The drive clears DRQ. If transfer of another sector is required, the drive also sets BSY and the above sequence is repeated from d).

6-6-1-1 PIO Read Command

a)	b)		e)			e)		
Setup	Issue Command		Read Status	Transfer Data	=====	Read Status	Transfer Data	
BSY=0	DRDY=1	BSY=1	BSY=0		BSY=1	BSY=0		BSY=1
			DRQ=1 Assert INTRQ	Negate INTRQ	DRQ=0	DRQ=1 Assert INTRQ	Negate INTRQ	DRQ=0

If Error Status is presented, the drive is prepared to transfer data, and it is at the host's discretion that the data is transferred.

6-6-1-2 PIO Read Aborted Command

a)	b)		e)	
Setup	Issue Command		Read Status	
BSY=0	DRDY=1	BSY=1	BSY=0	
			DRQ=1 Assert INTRQ	DRQ=0 Negate INTRQ

Although DRQ=1, there is no data to be transferred under this condition.

6-6-2 PIO Data Out Commands

This class includes:

- Format (50h)
- Write Buffer (E8h)
- Write Long (32h)
- Write Multiple (C5h)
- Write Sector(s) (30h)

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the drive to the host.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive / Head registers.

b) The host writes the command code to the Command Register.

c) The drive sets DRQ when it is ready to accept the first sector of data.

d) The host writes one sector of data via the Data Register.

e) The drive clears DRQ and sets BSY.

f) When the drive has completed processing of the sector, it clears BSY and asserts INTRQ. If transfer of another sector is required, the drive also sets DRQ.

g) After detecting INTRQ, the host reads the Status Registers.

h) The drive clears the interrupt.

i) If transfer of another sector is required, the above sequence is repeated from d).

6-6-2-1 PIO Write Command

a)	b)			e)			e)	
Setup	Issue Command		Transfer Data		Read Status	Transfer Data	Read Status	
BSY=0	DRDY=1	BSY=1	BSY=0 DRQ=1	BSY=1 DRQ=0	BSY=0 DRQ=1 Assert INTRQ	==== BSY=1 DRQ=0 Negate INTRQ	BSY=0 Assert INTRQ	Negate INTRQ

6-6-2-2 PIO Write Aborted Command

a)	b)		e)	
Setup	Issue Command		Read Status	
BSY=0	DRDY=1	BSY=1	BSY=0 Assert INTRQ	Negate INTRQ

6-6-3 Non-Data Commands

This class includes:

- Execute Drive Diagnostic (DRDY=x) (90h)
- Idle (97h,E3h)
- Idle Immediate (95h,E1h)
- Initialize Drive Parameters (DRDY=x) (91h)
- Check Power Mode (98h,E5h)
- Read Verify Sector(s) (40h)
- Recalibrate (1Xh)
- Seek (7Xh)
- Set Features (EFh)
- Set Multiple Mode (C6h)
- Sleep (99h,E6h)
- Standby (96h,E2h)
- Standby Immediate (94h,E0h)

Execution of these commands involves no data transfer.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive / Head registers.

b) The host writes the command code to the Command Register.

c) The drive sets BSY.

d) When the drive has completed processing, it clears BSY and asserts INTRQ.

e) The host reads the Status Register.

f) The drive negates INTRQ.

6-6-4 DMA Data Transfer Commands (optional)

This class comprises:

- Read DMA (C8h)
- Write DMA (C9h)

Data transfers using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel
- no intermediate sector interrupts are issued on multi-sector commands.

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- no intermediate sector interrupts are issued on multi-sector commands
- the host resets the DMA channel prior to reading status from the drive.

The DMA protocol allows high performance multi-tasking operating system to eliminate processor overhead associated with PIO transfers.

a) Command phase

1) Host initializes the slave-DMA channel.

2) Host updates the Command Block Registers.

3) Host writes command code to the Command Register.

b) Data phase - the register contents are not valid during a DMA data Phase.

1) The slave-DMA channel qualifies data transfers to and from the drive with DMARQ.

c) Status phase

1) Drive generates the interrupt to the host.

2) Host resets the slave-DMA channel.

3) Host reads the Status Register and Error Register.

6-6-5-1 Normal DMA transfer

Initialize DMA	Command
BSY=0	

BSY=1

DMA data transfer
BSY=x DRQ=x

Reset DMA	Status
BSY=1 nIEN=0	BSY=0

6-6-5-2 Aborted DMA transfer

Initialize DMA	Command
BSY=0	

BSY=1

DMA data
BSY=x DRQ=1

Reset DMA	Status
BSY=1 nIEN=0	BSY=0

6-6-5-3 Aborted DMA Command

Initialize DMA	Command
BSY=0	

BSY=1

Reset DMA	Status
BSY=1 nIEN=0	BSY=0

6-7 *Timing*

6-7-1 ATA Host Interface Timing Parameters

ATA Host Interface Timing parameters are shown in Table 6-12.

Table 6-12. ATA Host Interface Timing Parameters

Symbol	PARAMETER	TIMING			UNIT
		MIN	TYP	MAX	
TPW	DIORB/DIOWB- Pulse Width	10			ns
TRDA	DD Drive from DIORB asserted		25		ns
TWDS	Write data setup time to DIOWB	5			ns
TWDH	Write data hold time from DIOWB	5			ns
TRDH	Read data hold time from DIORB	20		70	ns
TADS	Address setup time to DIORB/ DIOWB	5			ns
TADH	Address hold time from DIORB/DIOWB	10			ns
TIOCSL	Address setup time to IOCS16B			15	ns
TIOCHL	DIORB/DIOWB asserted to IORDY			20	ns
TIOCHPW	IORDY- pulse width	25			ns
TIOCSH	Address hold time from IOCS16B	14			ns
THCS	CS setup time from IOCS16B	10			ns
THCH	CS hold time from DIORB/DIOWB	10			ns
TDDRQL	DIORB/DIOWB asserted to DMARQ			40	ns
TDACKS	DMACKB setup time to DIORB/DIOWB	0			ns
TDKA	DMACKB asserted to DD valid			28	ns
TADV	CS and DA valid to DD valid			25	ns
TMACH	DIORB/DIOWB hold time to DMACKB	5			ns
TDHT *	DMACKB negated to DD tristated				ns
TMWC	Multi-word DMA cycle time	120			ns

***** Applies at end of an ATA multi-word DMA cycle, when DMACKB is negated

6-7-2 ATA PIO Timing

ATA PIO Timing is shown in Figure 6-2.

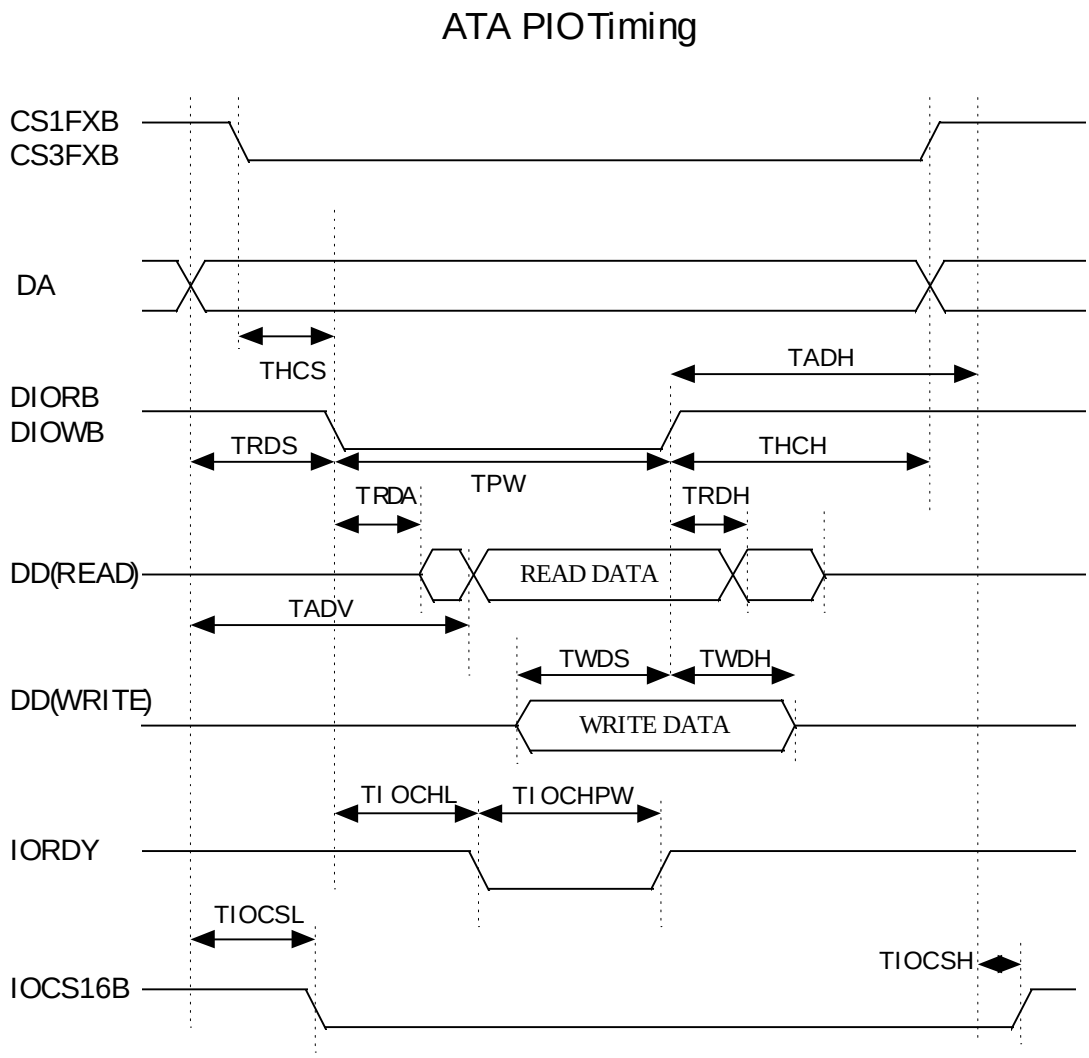

Figure 6-2. ATA PIO Timing

Chapter 7
MAINTENANCE

7-1 *General Information*

SAMSUNG's Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A hard disk drives achieve high reliability through their mechanical design and extensive use of microelectronics. Their designs allow fast, easy sub-assembly replacement without adjustments, greatly reducing the amount of downtime required for unscheduled repairs.

7-2 *Maintenance Precautions*

When servicing a drive, the service technician should observe the following precautions to avoid damage to the drive or personal injury.

(1) Do not attempt to open the sealed compartment of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A, as this will void the warranty and contaminate the media.

(2) Do not lift the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A by the PCB.

(3) Avoid harsh shocks or vibrations to the drive at all times.

(4) Avoid static discharge when handling the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A.

(5) Do not touch the components on the PCB.

(6) Observe the environmental limits specified for this product as listed in section 3.6.

(7) If it becomes necessary to move your computer system, turn off the power to automatically park the heads. Parking the heads moves the heads to a safe, non-data landing zone and locks the heads in place. This helps prevent the media and the heads from accidental damage due to vibration, moving or shipping. Do not move the drive for 20 seconds after removing DC power to ensure that the actuator is completely locked.

(8) Back up your data regularly. SAMSUNG assumes no responsibility for loss of data. For information about back-up and restore procedures, consult your DOS manual.

There are also a number of utility programs available that you can use to back up your data.

7-3 Service And Repair

The service and repair of the Winner 3A WA31273A / WA32543A / WA33203A / WA32163A / WA31083A, Winner 2A WA32162A can be done at a SAMSUNG Service Center. Please contact your representative for warranty information and service/return procedures.